# computing today

APR 1979
50p

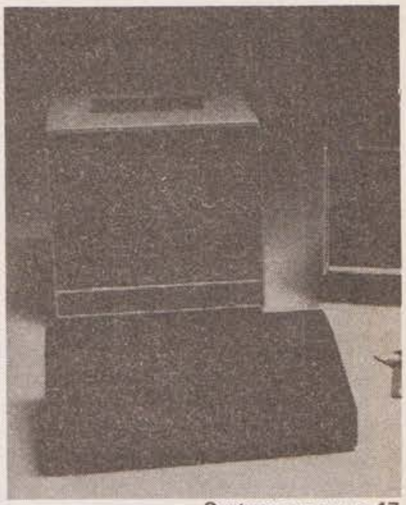
## HOME COMPUTERS: A SURVEY


**A TOUCH OF ASCII**
**S100 VDU PROJECT**
**NASCOM PACKAGE**

# computing today

VOL. 1 NO. 2
APRIL '79





System survey. p 47.



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## AN APPLE FIGHTS POVERTY
### Seth Dryden, Our US Correspondent Reports:

This is the story of two computers. One is a huge brute, the other is a dainty APPLE II. The general purpose computer (GP) operated by International Computer Systems in Coral Gables, Florida processes all prices and available data from over 700 retail food outlets, both small and large, to determine where the best bargains can be found.

The little APPLE II, on the other hand, is small enough to be transported around in the boot of a medium sized car. The APPLE's job is to disseminate the information in the most attractive way in order to coerce the hoi–polloi into eating better quality meals, and hopefully cheaper ones into the bargain. The project is being managed by the Community Centre in Miami on behalf of the US government. The area which concerns the authorities most are the two counties of Dade and Broward. Both are reputed to have a large proportion of Spanish speaking citizens as well as a high proportion of elderly inhabitants. The data for the project is culled from the two main newspapers that serve the region. The Fort Lauderdale News and the Miami Herald both carry up to 50 pages of food advertising a week, about 1,000 items. The advertising covers seven main food chains, including Winn–Dixie, Grand Union and A–G Great Value, as well as 25 independant markets and nine food co–operatives.

The GP computer has over 85,000 food items stored in its data banks, and this is updated week by week. Firstly sale items are analysed and printouts given of special offer items at each outlet with pricing as the main comparison. A weekly menu is then prepared based on 500 standard recipies. The next stage is a printout of the least expensive food item in all the categories. The final output is the production of a trend analysis to show whether the current prices are higher or lower than the previous week or indeed the previous time that the item was available. At this point the APPLE appears. Despite the main printouts being displayed at main libraries and also distributed through the mail free of charge there are still some areas that need up–to–the–minute reports. The APPLE can be used as a mobile terminal and is taken to shopping and high traffic areas along with its disk, printer and TV monitor to work on potential customers. As the least expensive items might not be shown to many people and some of the menus devised may not of heard of the APPLE is used to display digitized pictures of prepared meals, fruits and vegetables. The twin floppy disk system has a capacity of 116K and can run at up to 156K bits per second allowing a vast data–base to be maintained. The storage capacity allows for an index of vitamins, carbohydrates and the other nutritional factors from which the menu plans are formed.
The computer is powered directly from the car alternator as long as the engine is kept running to charge the batteries.

## COMPUTER CLUB ROUND–UP

A new computer club for those of you in the South London area has just been in contact with us. The club is known as SELMIC (South East London Micro–computer Club) and will meet on the third Wednesday of each month. The venue is the S. E. London College in Brakespeare Road, Lewisham Way SE4. They will have access to the full technical support of the college and are in the process of setting up specialised user groups. The membership secretary, Hugh Gilhespie can be reached on 01–303–4968. The next meeting is on the 25th of April between 6.30 and 9.00pm.

We've recently heard of the formation of the Hull and District TRS80 users group. The club meets on the second Tuesday of each month, for further details contact Frederick Brown, 421 Endicke Lane, Hull, Yorkshire. If anyone else has plans to start a club please let us know, and to any established groups please keep us posted on your activities. Write to Computing Today, 25–27 Oxford Street, London W1. . .

An MK14 and SC/MP micro–processors user club is being formed in the North London area. For further information please contact Mr. G. Phillips at 8 Poolsford Road, London NW9.

The East London Amateur Computer Club held it's third meeting recently. A TRS 80 and a Nascom 1 were the main attractions and a short talk was given about each machine. Afterwards members were given the opportunity to discuss their own systems. Future meetings will include demonstrations by manufacturers and a members only meeting at a local computer shop. Anyone interested is welcome to come to the meeting room at the Harrow Green Library in Cathall Rd., Leytonstone, between 7pm and 10pm on the third Tuesday of the month. For more details contact Jum Turner, 63 Millais Rd., London E11.

We have heard from the secretary of the Bristol Computing Club that they have now established a regular meeting on the third Wednesday of each month. Anyone interested in obtaining further information should contact the Chairman, Mr. L. Wallace at the following address: 6 Kilbernie Road, Bridge Farm Estate, Bristol. BS14 OHY

Please enclose an SAE to assist prompt reply.

## NASCOM ADD–ONS

A range of accessories has been announced for the NASCOM by Jeff Wayne Music (Electronics) Ltd. The currently available units are a graphics kit which plugs into the character generator socket on the NASCOM and then forms the interface through which the other units may connect. These are a 1K programmable graphics board complete with colour TV video matrix, D to A and a video modulator. The PAL encoded output may be connected to the aerial socket of a TV. A second channel input may be used to provide sound from the TV's own speaker. This sound input may be driven from another accessory, a programmable sound effects generator. This can also be used to control an external synthesiser. Further product shortly to become available will include a programmable CRT controller. This will feature memory mapping, up to 8 pages of 2K characters and a light pen option. Also on future release will be a house controller/monitor, featuring a real time clock display, the facility to drive up to 4 solid state relays directly and two D to A converters. This unit will be supplied as a self contained system with the possibility of connecting to a central processor. Another very useful goodie that the firm offer are Machine Code programming sheets . These are supplied in A4 pads of 100 at £1.75 each.

## SERIAL CONVERTER

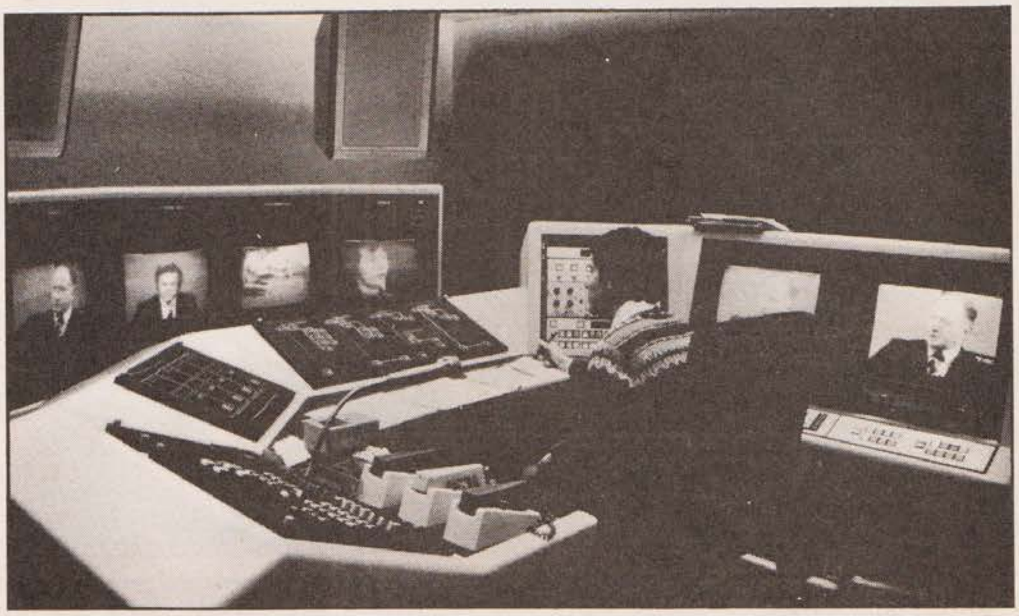
A low–cost V24/20 mA converter has been announced by Shade (Computer Services) Ltd of Calne, Wiltshire. The unit allows V24 devices to be driven from 20 mA or vice–versa. Data rates of up to 9600 Baud can be handled by the device which is available as a free standing unit or as an 8 channel rack–mounted unit. Shade may be contacted on Calne 815757.

## GEC EXPAND IN VIEWDATA MARKET

GEC Computers will have supplied over £10M worth of 4000 series machines for Viewdata useage both at home and abroad in the year ending 31st March. The British Post Office has expanded its system from 5 to 31 4000 series computers to be used on the Prestel system. Foreign orders include West Germany, Switzerland, Holland and Hong Kong, all of which are setting up Viewdata systems, both private and public.

## FERRANTI FOR IBA REMOTE CONTROL

Ferranti Computer Systems have won a £½M contract with the IBA to supply four Remote Control and Super-visory Systems. These will enable remote operation of unattended transmitter sites in Yorkshire, South Wales, Central Scotland and Croydon. Each region will be equipped with dual Argus 700G minicomputers semiconductor memory and cartridge disk backing store. Specially designed master stat-ions will interface with the existing telemetry control sys-tems. The units will be able to monitor equipment and ass-ume remote control when nec-essary. A further feature is that they will be able to pass information to maintainance bases should remedial action be required.



## VIEWDATA ON 6800

A new 6800 based computer system has been announced, but this one has one rather special feature that makes it stand out in the field. The system is called TECS and has been announced by a Liverpool based firm, Technalogics. The outstanding feature is that it is designed around the Teletext system and thus not only does your TV act as the display for the computer but also as a fully decoding Teletext system. It caters for all the latest addit-ions such as double height and background colour. The CPU will also run a resident mini-BASIC and this has access to the full Teletext character and graphics set. We will review the machine in greater detail in next months issue. The cost of a minimal system is expected to be around £450 but kit versions will be available.

# NEWS

## HIGH QUALITY DAISY PRINTER

The latest Qume 'Daisy–wheel' printer is now being brought into the country by Facit Addo Ltd., of Rochester.A regional dealership network is being set up to provide a full service to the purchaser on a country wide basis. The new model, the Sprint 5, is available as a terminal or as just a printer at prices from £2,150. Baud rates of 110 to 1200 are available along with a variety of interface options. The printer can be used under software control providing for bi–directional printing and variable pitch with proportional spacing. There is a wide range of type–faces available to cover most applications from scientific to small business use.

## EXHIBITION NEWS

Computermarket '79 is touring the country at the moment and will be in London at the Bloomsbury Centre 3–5 April. Previous venues are Glasgow, Birmingham and Manchester. The exhibition is open FREE to all business people over 18. For further information contact the organisers on 01–437–4187 . . .

An International Word Processing Conference and Exhibition is being held at the Wembley Conference Centre from 10–13 July this year. Claimed to be the only one of its kind this side of the sea it is intended to provide a showcase of available equipment and there will be a series of half day seminars to introduce people to the ideas. For further information contact Online Conferences Ltd., on Uxbridge 39262.

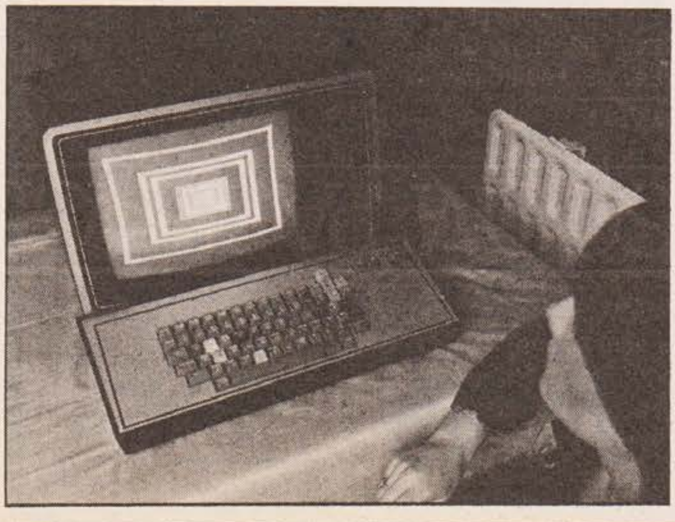
## MARCONI TO SUPPLY VOICE RESPONSE TO THE CAA

A new automatic Voice response system has been supplied to the CAA by Marconi Space and Defence. The system will provide an automatic weather forecast service for the Volmet system. The service supplies an up to date weather report for pilots from data which is received at the Civil Aviation Communications Center at Heathrow Airport. The data is received by Telex every half–hour and the new system will decode and use the information to control a data bank of encoded words and phrases stored in computer memory. This is transmitted on up to four frequencies on a continuous basis. Further applications for this type of system include railway time–tables and road reports.

## ADD–ON FOR PET, NEW KEYBOARD

An add–on keyboard has been announced by Northend Office Supplies Co of Essex which can be used with the PET. This is a standard keyboard with the addition of the six control keys and sits in front of a PET. The unit works in parallel with the built–in keys so that you can now type fast and still use the graphics when you want. The price for a cased model is £89.50 but it is available as a "naked" unit for £69.50.

## COMPUCOLOUR ARRIVES AT LAST



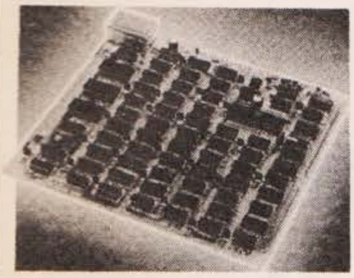
The long awaited COMPU–COLOR II personal computer has at last come to these shores. Abacus Computers Ltd., will be distributing it and dealerships have been arranged with Byte shop and Trans–Am. The Model 3 is supplied with a 13" 8 colour VDU, 72 keyboard, built–in mini–floppy and 8K of user RAM. The machine has been considerably tidied–up in appearance since we last saw it and now includes 16K extended disk BASIC, 51.2K bytes per side of disk and the VDU now handles 32 lines of 64 charac–ters. The price of this little lot is £1,390 and you get a floppy containing programs thrown in as well. If you want expansion (who doesn't) 16 and 32K versions are available along with 101 and 117 key expanded keyboards.

## 80 COLUMN PRINTER

An 80 column bi–directional printer is being marketed by Dataplus of Cheltenham. It can be supplied with full electronics to accept a parallel or serial ASCII coded input and can run at speeds of 100 cps. A dot matrix head is used, either 5x7 or 9x7, and the paper can be friction or tractor fed. A special condensed 7x7 matrix head is also available to increase to capacity to 96 columns. The ribbon is supplied in a cartridge so you don't get messy fingers. The cost of the basic model is around the £250 mark which compares very favourably with the currently available models.

# TANGERINE

**COMPUTER SYSTEMS LIMITED**



NEW! READY BUILT MODULES NOW AVAILABLE IN 7 DAYS, KITS FROM STOCK

A fully compatible terminal when used with a keyboard and domestic TV (or monitor), that can replace any serial terminal for a fraction of the cost.

Apart from the regular features that most VDUs have, the 1648 can perform the following;

★ Fully controllable cursor.
★ Generates 16 lines of 44/48 (selectable) characters in both upper and lower case with any keyboard, even those **without** an 'alpha' facility.
★ Break and repeat also provided.
★ RS232 and full current loop I/O provided.
★ Full control character decoding – selectable by the user to perform cursor movements, bell, page clear, and for switching any other peripherals with suitable interfacing.
★ 10 switchable Baud rates.

All VDUs are supplied with an A4 size ring binder containing 50 pages of comprehensive manual with large A3 fold-out Circuit Diagram and Component layout. Details of graphics, and other applications are also included.

**COMING SOON!**

We shall be announcing soon the details of our Professional Keyboard available in both kit and ready built versions, with a numeric pad option. Reed keys are used exclusively, it is therefore exceptionally reliable and robust.

Other products to be announced are:

★ **Z80** based single-board microcomputer.
★ **6800** based single-board microcomputer.
★ **& CRT Controller,** an economy VDU module using software to control its functions – also Teletext compatible, with full graphics.
★ **Add-on Graphics module** for the 1648.
★ **Add-on Hex Keypad,** for machine coding.
★ **Add-on** μ modem, for cassette interfacing.
★ **Prom Programmer.**
★ **Complete monitor-less terminal.**

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Rivermill Lodge, London Road, St. Ives, Huntingdon, PE17 4BR. Tel: 0480 65666.

Please send the following,

☐ Further information.
☐ 1648 VDU Kit at £129.50 inc. pp + VAT £10.36.
☐ 1648 VDU Built and tested at £154.50 inc. pp + VAT £12.36.

Name: ..........................................

Address: ..........................................

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Business telephone: ..........................................

Home telephone: ............... Date: ..................

I enclose a cheque No: ............ for the sum of .........

£............ INC VAT.

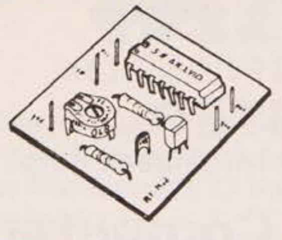
Signature: ..........................................

Overseas customers should send a bank draft on a London Bank. Include sufficient postage for air/surface mail for 1·3 Kg.

# LOW COST R.F. MODULATOR

## Only £ 2.—

**includes p.&p.!**



Converts ordinary T.V. into Video-Monitor. Use it for computing or video-games. This board has a special Video-IC and is easy to build (ten minutes). No special adjustments, works always. Tuning by turning potentio-meter.

Low Power 5 volt. Kit includes all parts, epoxy p.c. board and assembly instructions written in English.

**How to order: Send your order and remittance to the address below. Or, send us your undersigned Barclays or Eurocheque for a value of £2.**

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**P.O. BOX 410**
**ARKELSE ONDERWEG 31**
**4200 AK GORINCHEM**
**THE NETHERLANDS**

**Your video R.F. Modulator will be shipped the same day we receive your order**

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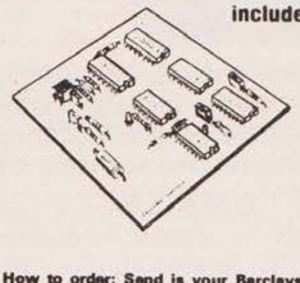
# LOW COST CASSETTE INTERFACE

**includes p.&p.! Only £ 8.75**

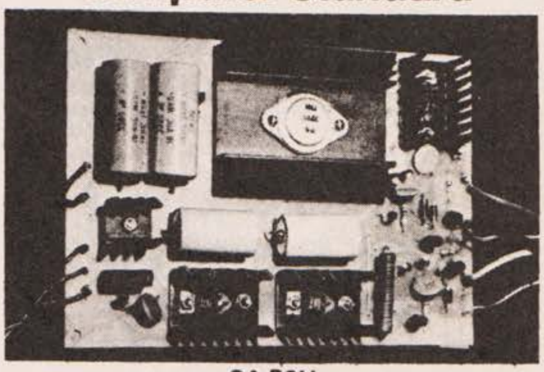


Convert your cassette-recorder into a digitalrecorder. Easy to build, no adjustments! Uses Kansas City Standard. High speed, till 1200 Baud. Full Duplex, which means that you can (if neccessary) use the interface with 2 cassetterecorders at one time. Audio in- and outputs connects directly to cassette-recorder. Data in- en outputs are T.T.L. compatible. Low Power, only 5 volt needed. Kit includes all parts, heavy epoxy p.c. board with edge connector and clearly written manual in English. Board also available assembled and tested for £ 11.75 incl. p.&p.

**How to order: Send is your Barclays, Eurocheque or other remittance in an envelope, put your name in capitals on the back. Kit £8.75 includes P&P. Assembled and tested (guaranteed for 90 days) £11.75 incl. P&P. Send your order to: Musicprint Computer Products b.v., P.O. Box 410, ARKELSE ONDERWEG 31, 4200 AK GORINCHEM, THE NETHERLANDS. Phone 010-31 18 30-24693. Your cassette interface will be shipped the same day we receive your order.**

**dealer inquiries invited**

# Computer standard



**3A PSU**

Computers require a reliable and even power supply. The redesigned and uprated Nascom 3A PSU meets these requirements. Its output voltages are +5V 3A; +12V 1A; –12V 1A; –5V 1A. And are sufficient to drive the Nascom–1, buffer board and up to 32K of RAM. It has LED displays on all the outputs and will fit into the Nascom frame to be announced soon.

Price of PSU kit–£24.50 plus VAT.

A buffer board kit with edge connectors suitable for the NASBUS and with edge connectors and interconnectors to attach directly to the Nascom–1 is available at £25.00 plus VAT.

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# Star Devices Limited

## Low cost ASC II Encoded Capacitive Touch Keyboard

**now with improved sensitivity**

# £37.50

including V.A.T., post and packing.
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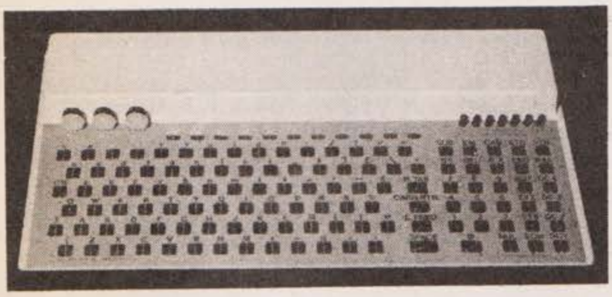

The Standard Unit Offers: —

- ★ 7-bit parallel ASCII encoded output.
- ★ Positive and negative strobe edges.
- ★ All code outputs will drive 4 TT loads.
- ★ LEDs to show code of selected character.
- ★ Audio feedback with volume/tone control.
- ★ Adjustable output character rate.
- ★ Touch-pad sensitivity control.
- ★ Sensitivity control.
- ★ Auto-character repeat.
- ★ Automatic scan facility.
- ★ Requires 5 volts at only 200mA.
- ★ Gold-plated edge connector provided.
- ★ Rugged low-profile case.
- ★ Assembled, tested and burnt-in.
- ★ 6-month guarantee.
- ★ All 128-character ASCII set.
- ★ Comprehensive Handbook supplied.

Low-cost optional extras include
- ★ Serial RS232 ★ Baud rate and +12V generator
- ★ Parity check bit ★ On-board 5V regulator
- ★ 20mA current loop ★ 30V open collector output active high or low

For further details please write to: —

**STAR DEVICES LTD.,
P.O. BOX 21,
NEWBURY,
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OEM and Custom design inquiries welcome.
Overseas distributors wanted.

# 'MERCURY'

**Basic system prices start from £650** (+VAT). Contact Mr. Seton at **P. & R. Test at Maldon (0621) 57440** for further information.

P. & R. Test announce the "Mercury" microcomputer, for home and office use: based on the advanced Z.80 CPU chip, in conjunction with the well-proven IBM Golfball printer and a solid-state keyboard, the basic system comes with 2K or ROM containing the Monitor and I/O routines, 1K of user RAM, 1 1K PROM sockets which will accept Tiny Basic, and 2 serial interfaces — it is intended that one of these be used to interface to an external line (20 mA loop, or EIA levels) and the other to a cassette recorder, though this assignment can be changed by the user. System expansion options include a VDU, which is memory mapped on 1K of RAM and requires only a small-screen TV or monitor (also allowaing the RAM to be used as normal memory by turning the VDU "off"), memory expansion from 4 to 32K of dynamic RAM, an Editor/Assembler (ZEAP) using 3.5K of RAM, a high-level language (8K BASIC) on a ROM board, and a floating-point processor. Also under development are a speech synthesiser, a floppy disc system, a low-cost 100Mbyte disc drive and controller, and a Teletext/colour graphics processor.

**P. & R. TEST announce the Mercury Microcomputer for home and office use.**

## Written for the Nascom

Among the programs written to run on the Nascom—1 and available now are:

**ICL Dataskil Letter Editor**

This software provides a comprehensive set of data operations. Text can be input, displayed, edited, stored on tape, retrieved and further amended. Control functions include cursor, character, word, line, scrolling, tabbing, tape store and retrieve, text printing. All in less than 2K byte plus workspace for up to almost two full screens. Price on 2 x 2708 EPROM £70 plus VAT.

**TINY BASIC**

A 2K BASIC Interpreter in 2x2708 EPROM. Normal commands: 1—32767 MSL/single array/arithmetic constant/ <>≦≧=≠ /strings valid in PRINT/supplied with user manual/additional three level keyboard control/compatible with NASBUG and B.Bug Price £25 Plus VAT.

An extended version of the above is our SUPER TINY BASIC which has all the TINY BASIC functions plus full editing features and additional operator command. Price in 3x2708 EPROM £35 plus VAT.

**ZEAP**

An editor assembler which runs under NASBUG and provides the powerful advantages of writing programs in Z80 assembly language instead of directly in machine code. Uses less than 3K bytes of memory and is supplied on cassette priced £30 plus VAT.

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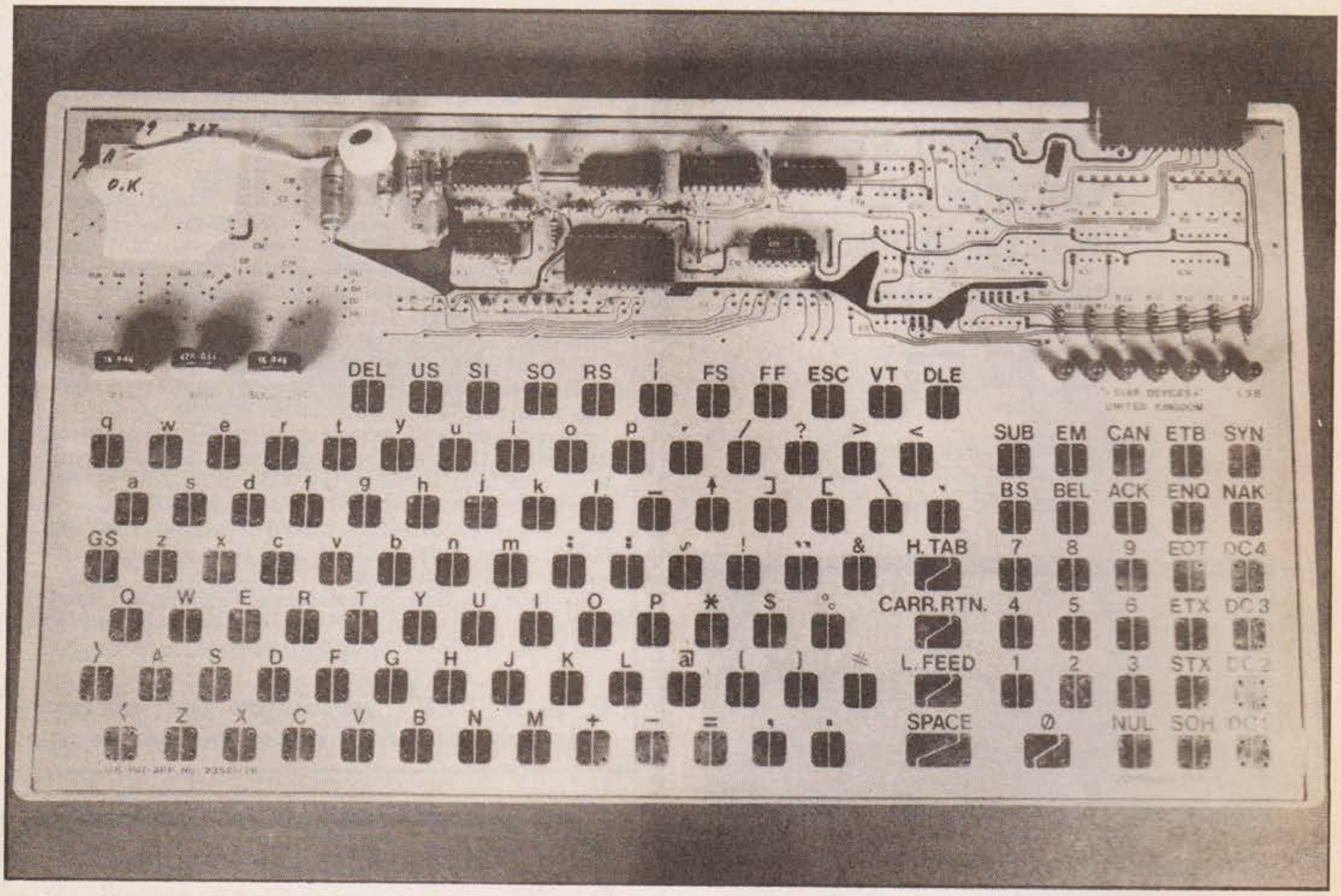



**The interior view of the keyboard unit. The audio bleeper can be seen at the top right, and below it are the adjustment pots used in the setting up procedeure. The edge connector at the top right is supplied with the unit. The LED's display the ASCII code sent by the keyboard, very useful for setting up the unit.**

A new low cost ASCII keyboard has recently been ann—ounced by STAR DEVICES of Newbury. The unit is supplied ready built and features a 128 pad capac—itive touch keyboard. In its basic form the unit provides a seven bit parallel output at TTL levels with both positive and negative strobe. We decided to take a closer look at this device to see how it compares with the more conventional keyswitch type of peripheral, at £37.50 it is about half the price of a standard unit.

### Getting The Feel.

As the unit is touch sensitive we followed the setting—up instructions given in the comprehensive instruction manual very carefully. To facilitate the setting up an audio tone is produced each time a key is registered as being struck, with the code corresponding to this key being displayed on a row of LED's mounted at the top right (see photo 1).

By using both of these facilities the keyboard may be rapidly adjusted for personal touch by means of two small pots mounted at the top left of the unit. These control the sensitivity of the pads and the rate at which the character is accepted. By keeping one's finger on the pad an auto—repeat occurs, thus the rate should be adjusted so that a reasonable delay is incurred or else double characters will be sent.

### How It Handles.

To prevent the loss of any facilities all the ACSII codes have a dedicated pad 128 of them. This means that you have both an upper and lower case QWERTY layout with a separate numeric pad. The other standard characters such as .,+ etc are distributed around the keyboard area along with the control keys such as FF for Form Feed (Control L).

All these control keys are documented in the back of the handbook along with the rest of the ASCII set, a very useful list to have. With all these pads on the keyboard, clearly labelled though they are, it takes quite a bit of practice to type with much more than two fingers, although it is much better than the old pet keyboard. Dirt on the keys, or moisture, does not seem to cause false triggering but it can cause difficulty in getting a trigger from the key. The manufacturers supply a rubber for cleaning the keys with and this solves the problem.

### Connecting Up To The World

As the basic model the keyboard comes with a 7 bit parallel interface at TTL levels and a strobe, both positive and negative phases are available. The strobe signal goes high when valid data is present for the length determined by the

# STAR KEYBOARD REVIEW

data rate pot. This simple output should be easily interfaced with any parallel input port. An optional parity bit is available to give the full 8 bit code.

### Keeping Your Options Open

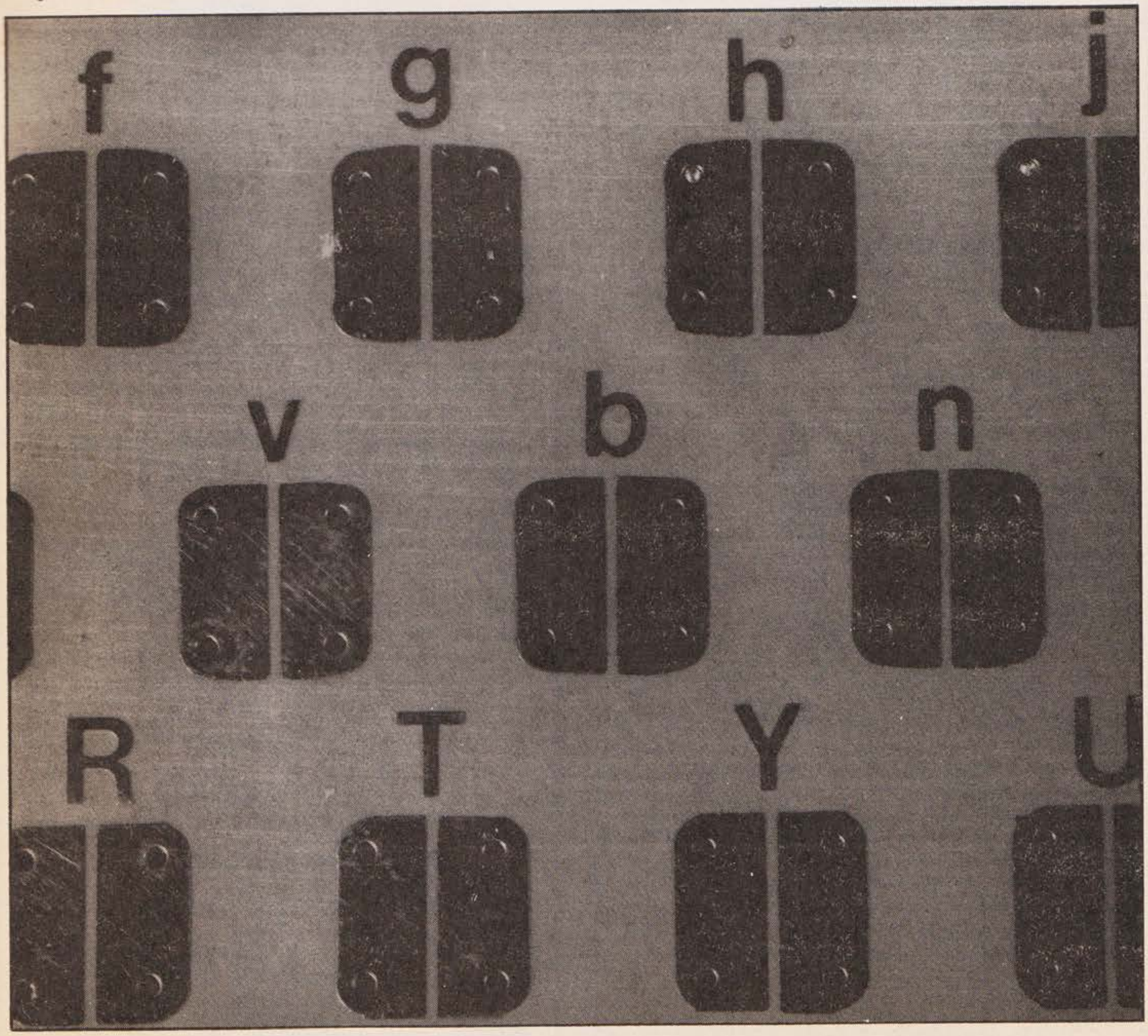
The number of options offered for this keyboard mean that you should have no trouble at all fitting it into any system. Various serial interfaces are available, RS232, V24 and 20 mA current loop, (for those confused between these see our up–coming article.) As each of the above requires a clock an internal Baud rate generator is available as is on–board voltage regulation. For the parallel interface an on–board 5 V regulator is available along with active low outputs.

A further option is a 30 V open collector output available in either active high or low. If you can't interface to one of these options then you must have a very odd device indeed! One rather interesting feature supplied as standard, but optionally connected, is a patch on the rear edge connector which sends each ASCII character twice then sends the next twice, e.g.. aabbcc etc., very useful for testing interfaces among other things.

### What Goes On Inside

We had a careful look inside our unit, they are supplied sealed and you invalidate the warranty if you open it, which was supplied open. As you can see from the photo it is

**A close up of the actual keypads revealing the clear labels which are actually etched as part of the PCB. The whole surface is tinned to give a long trouble–free life.**



# STAR KEYBOARD REVIEW

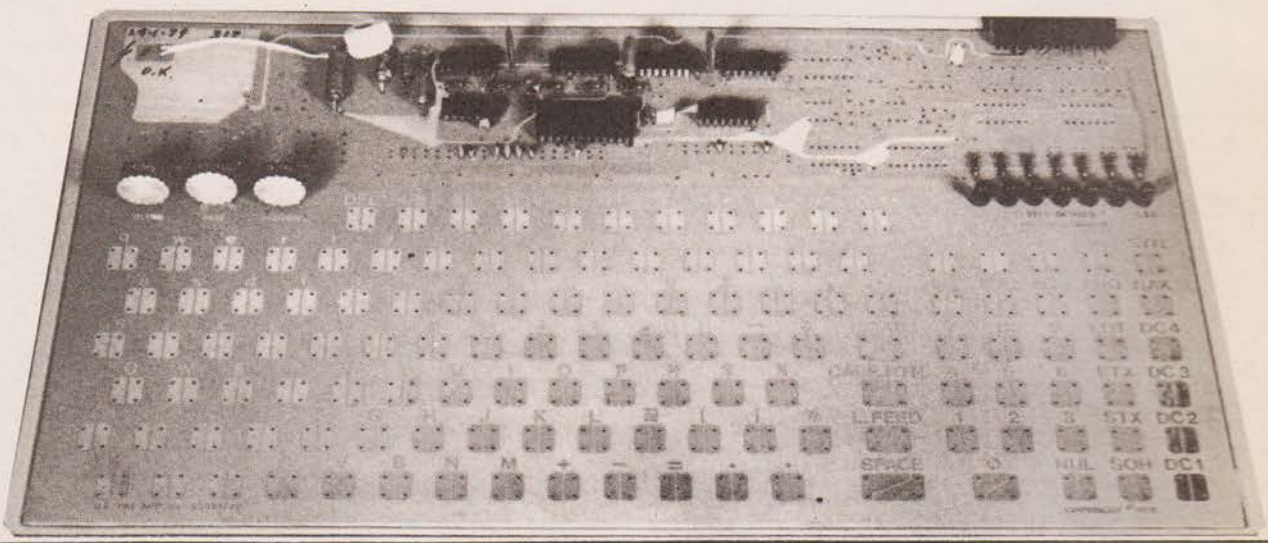
fairly simple. There are only 7 TTL chips in the basic model, the blank areas seen in the internal picture (photo2) are for the various options.

The designer is in the process of obtaining a patent for the circuitry and so we are not at liberty to disclose the actual workings but suffice to say that the basic idea is very simple and very effective. The use of standard TTL should give good reliability to the unit at not too unreasonable a current consumption, 200 mA.

**The opened unit, revealing the double sided PCB which acts as the keyboard as well as carrying the necessary circuitry. The spare IC positions are for holding the variety of options available.**

**Summary**

This keyboard should provide a very reasonable low—cost alternative to a standard key—switch type and can be easily interfaced to any system. Further advantage is obtained by having all the ASCII codes available on a single pad, often the CONTROL key is not supplied as a standard on commercial units. The only slight disadvantages are the key layout which takes a little time to get used to and the fact that fast typing is rather difficult although the two—key rollover does help. All in all a useful piece of equipment at a reasonable price, and British to boot.



By Roger Bird:

```
                    A/L ACCOUNT
==============================================
I        Item              I   DEBIT  I BALANCE I
==============================================
I                          I          I  144.78  I
I     FARES                I   65.00  I   79.78  I
I     ACCOMODATION         I   53.50  I   26.28  I
I     INSURANCE            I    8.25  I   18.03  I
I     ENTERTAINMENT        I  180.00  I - 161.97 I
I                          I          I          I
I                          I          I          I
I                          I          I          I
I                          I          I          I
I                          I          I          I
I                          I          I          I

Enter ',' for Index '/' for finished
```

**Figure 1.**

One of the challenges presented by computer programming is to compile a program which fulfills an idea, incorporating as many facilities as possible within a given RAM space. One such idea was to create a program which would assist in the organisation of a personal budget. It was to contain ways of ensuring that forthcoming bills would be provided for and give an indication of It MUST remove the possibility of being able to make arithmetic errors.

The idea was simple enough. The total outgoings would be split into groups. Those that could be covered by standing orders or budget accounts were, leaving only day to day running costs to deal with. Each account was analysed to determine its annual expenditure. This was divided by 12, thus giving a minimum monthly input requirement.

A running budget of each account was to be kept by the computer and items could be credited or debited as required. The resulting balances being stored on magnetic tape for future reference, and the all important money is being kept in a building society gaining interest and being withdrawn only when required.

### The Program

An explanation of the program will be brief as the listing and flowchart should be self explanatory. It is reccommended that the tape control relay be fitted as not only will it provide full automatic control under this program but will make life easier when running any load or dump routines. The program should be executed from address 0C50 and this will arrange for the latest balance figures to be entered. When the balances have been entered an index is printed on the screen using the 'print line and scroll' technique. There are 7 lines and each contains the title of two accounts as shown in locations E00 to E68. There is nothing magic about the names except that they all have different starting letters, a fact which is exploited in locating the correct balance register. It should also be noted that where there are an odd number of titles the line is balanced with an additional stop command (E68).

To enter the required account the initial letter is typed. This is recognised and in its ASCII form is used as the lowest significant byte of a table address. The table is contained in addresses 0F41 to 59. If for example the A of A/L is typed the ASCII A (41) is used and the address 0F41 is interrogated. The contents (BD) are combined with the highest address byte of 0F to point to the register address, i.e. 0FBD. The first location of this register contains another reference vector, in this case 45. This when combined with a highest byte value of 0E points to the title address 'A/L'. This reference back allows the titles which are expensive on RAM to be utilised as both index and account heading.

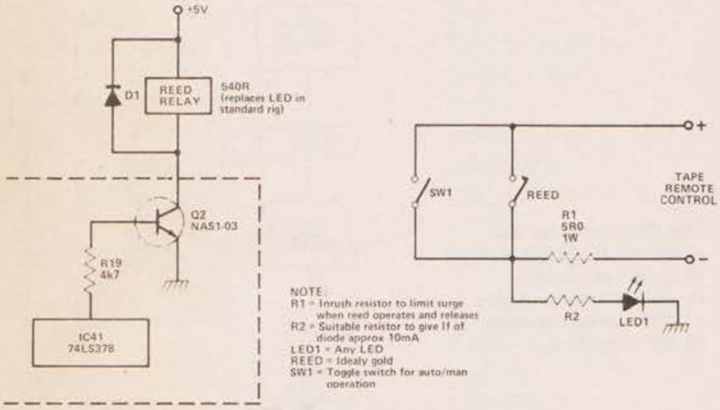
Once the account has been selected the tabloid is printed, again using the 'print and scroll' technique. The format of the tabloid is shown in Fig 1.

Once the tabloid is printed the lettering is added using memory mapping methods and the current balance is read onto the screen from the register.

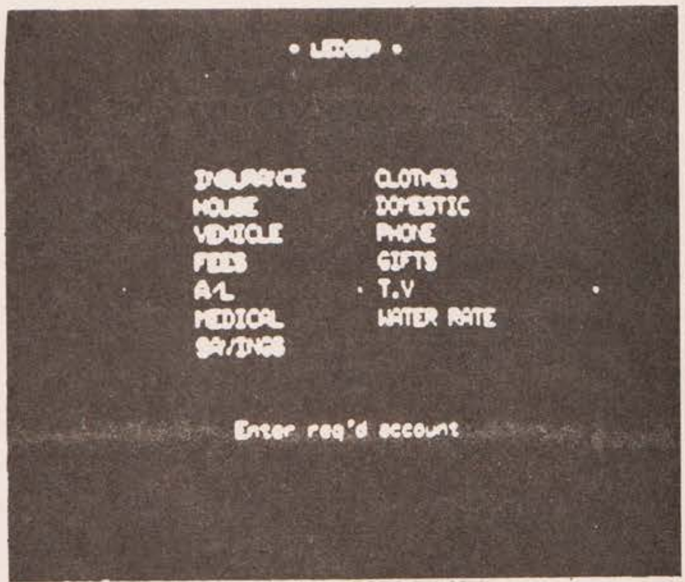
Next the question is asked 'CREDIT DEBIT OR INDEX ?'. If INDEX, it assumes that no changes are required and returns to the index routine for the next account. If CREDIT or DEBIT, the appropriate word is printed on the screen and address 0F24 is set to either 'add C with carry' or 'subtract C with borrow' thus initialising the arithmetic routines.

The program now waits for further entries as follows:-

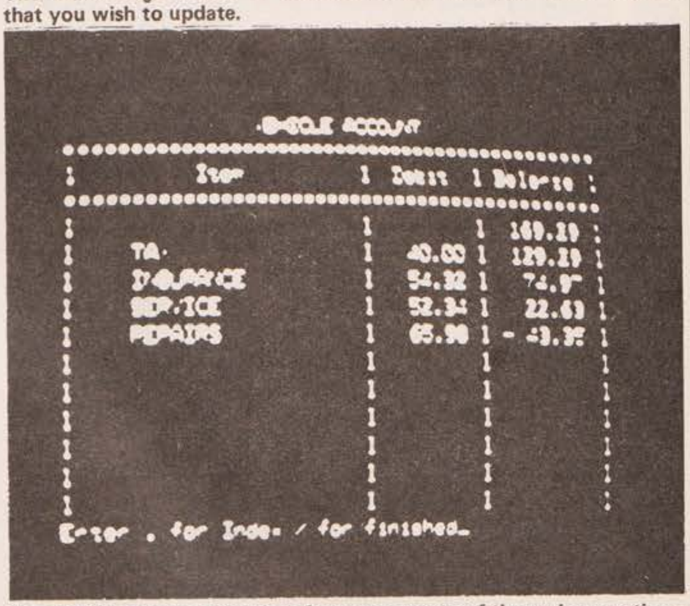
| | |
|---|---|
| Any letter | This is printed in the item column and the CRT address stepped on. |
| Any number | This is considered as the unit pence figure. The existing item amount is shifted one place to the left and the unit pence figure inserted. Note that the decimal point is automatically aligned. It is therefore necessary to enter both the pounds and pence. |
| B/S | This will delete a whole line, both text and amount. The CRT will reset to the beginning of that same line. |
| N/L | This assumes that the entry is correct. The ammount is totalled to the balance which will be printed in the balance column. The CRT will be set to the beginning of the next line. |
| , (comma) | Here the program recognises that all entries have been made. The CRT is cleared and the index reprinted. Only the current balance is retained in the registers. |



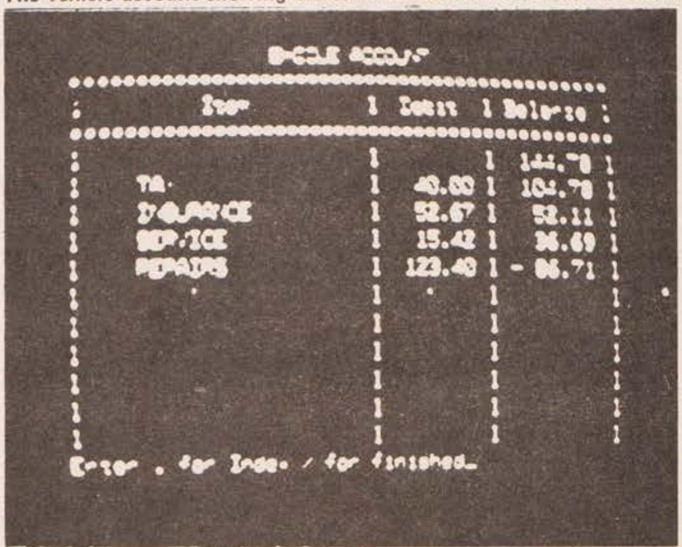

**Circuit for the NASCOM tape recorder automation.**




**The main ledger index of accounts, from here you select the one that you wish to update.**



**The vehicle account showing the current state of the various sections.**



**The vehicle account after an update has been done, note the changed totals and final balance.**

/ (slash) — All entries have now been completed and the registers are ready for storage on the magnetic tape.

The parameters of the program are a maximum register capacity of £8999.99 and a minimum of £-999.99. When printing the balance the program looks at the highest digit and tests for a 9. If a 9 is present it assumes the number to be negative. The balance is then converted in a tempory register from HEX negative numbers to decimal and is copied from there to the CRT. All the leading zeroes have been blanked except when the balance is less than £1. Then a zero is put in the pounds column for aesthetic reasons.

### Program and Register Storage

Long term storage is achieved by using magnetic tape. Initially the program only locates 0C50 to 0F84. At the completion of an 'update' on pressing the '/' key the CRT states, 'SWITCH TO REC AND UPDATE LOG', 'READY? TYPE YES'. When YES is typed the program looks for S and starts the tape running. The registers 0F85 to 0FDF are then dumped onto the tape. This entry should be logged as A. When the program is next used the latest entry will be A, so on the completion of loading the tape will be standing at the end of the first recording of the registers. Thus the next dump should be logged as B etc.

### Special Features

If you've studied the listing you are probably baffled by the addresses 0C71 and 0C74 to 76, as these appear to do nothing useful or call for an entry that does not exist. The explanation ? The NASBUG T2 does not, for some inexplicable reason, like having the load routines used in user programs. These locations have been designed to fool the monitor, and what's more the program won't run without them.

### Program Changes

Many personal computer owners will want to use their own account titles and this is catered for as long as they begin with different letters. What must be remembered is that the Table and the initial register vector MUST be changed accordingly.

This program is designed to carry out the debit and credit functions on a personal ledger of 13 seperate accounts. The registers at the end of the program are dumped on completion of a series of entries and can be recovered seper–ately if required. This provides both continuity and error protection. Each page is handled seperately for debit and credit entries requiring seperate access through the index. Decimal points are self–aligning and should not be entered, however it is always necessary to enter pence. Entries are labelled A–Z.

EXECUTE FROM C50

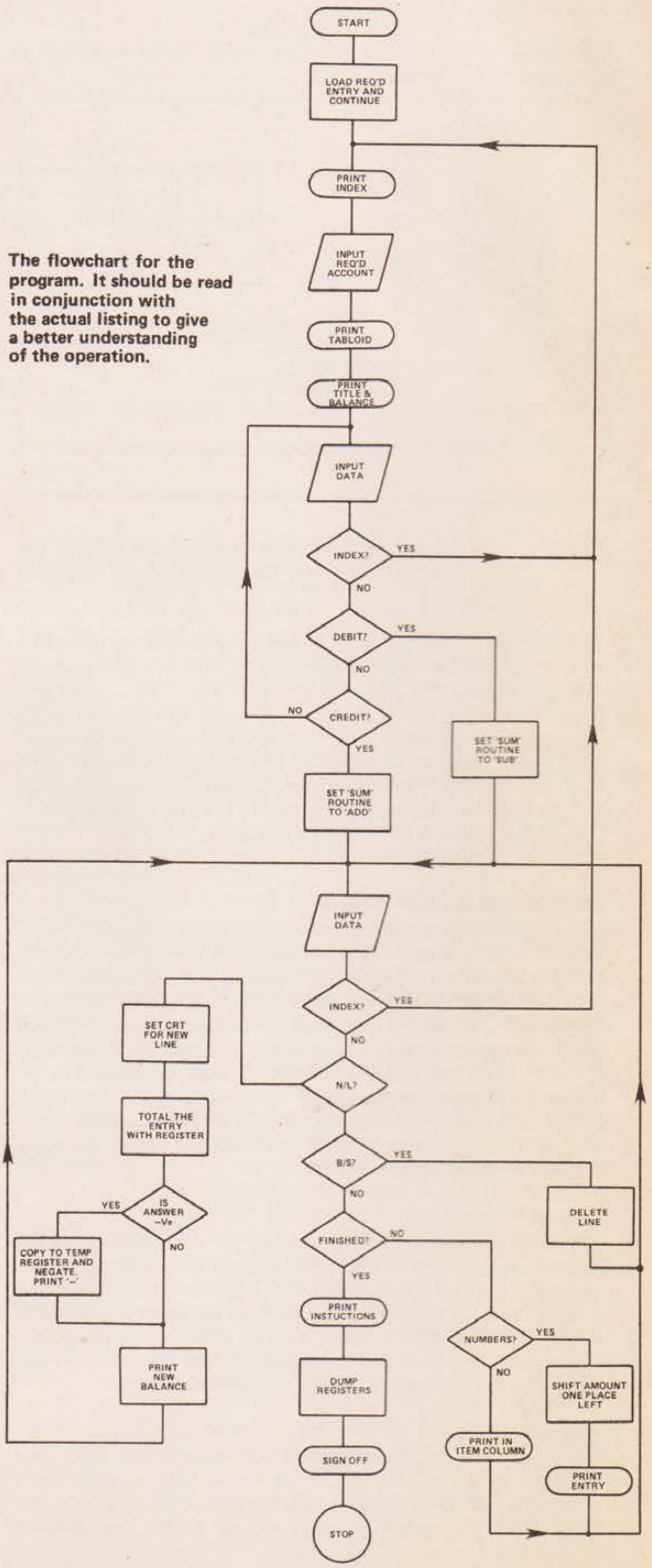
```
C50  EF                'LOAD'      RST 40
C51  1E
C52  WHICH ENTRY?                  TEXT
C5F  00
C60  CD 3E 00                      CALL CHIN
C63  CD 3B 01                      CALL CRT
C66  D6 40                         SUB 40
C68  47                            B , A
C69  CD 40 02                      CALL CRLF
C6C  C5                'LOAD 1'    PUSH BC
C6D  CD 7C 03                      CALL LOAD
C70  C1                            POP BC
C71  35                            DEC (HL)
C72  10 F8                         DJNZ 'LOAD 1'
C74  CD 3E 00                      CALL CHIN
```

PRINT INDEX

```
C77  EF 1E 00          'INDEX'     RST 40
C7A  11 DB 0B                      DE=0BDB
C7D  21 00 0E                      HL=0E00
C80  CD 35 0F                      CALL PRINT 1
C83  06 07                         B=7
C85  1E 93             'INDEX 1'   E=93
C87  CD 34 0F                      CALL PRINT
C8A  1E A2                         E=A2
C8C  CD 34 0F                      CALL PRINT
C8F  CD 40 02                      CALL CRLF
C92  10 F1                         DJNZ 'INDEX 1'
C94  EF 1F 1F 00                   RST 40
C98  1E 96                         E=96
C9A  CD 34 0F                      CALL PRINT
C9D  E5                            PUSH HL
C9E  CD 40 02                      CALL CRLF
```

SELECT ACCOUNT AND PRINT HEADER

```
CA1  CD 3E 00                      CALL CHIN
CA4  6F                            L , A
CA5  24                            INC H
CA6  6E                            L , (HL)
CA7  E5                            PUSH HL
CA8  D9                            EXX
CA9  E1                            POP HL
CAA  6E                            L , (HL)
CAB  25                            DEC H
CAC  11 DA 0B                      DE=0BDA
CAF  CD 35 0F                      CALL PRINT 1
CB2  E1                            POP HL
CB3  CD 34 0F                      CALL PRINT
```




The flowchart for the program. It should be read in conjunction with the actual listing to give a better understanding of the operation.

```
PRINT TABLOID
CB6  CD 5B 0F              CALL LINE
CB9  06 02                 B=2
CBB  CD 76 0F              CALL GRID 1
CBE  CD 5B 0F              CALL LINE
CC1  06 0C                 B=0C
CC3  CD 76 0F              CALL GRID 1
CC6  11 55 08              DE=0855
CC9  CD 34 0F              CALL PRINT
CCC  1E 6F                 E=6F
CCE  CD 34 0F              CALL PRINT

PRINT BALANCE
CD1  D9                    EXX
CD2  23                    INC HL
CD3  11 EF 08              DE=08EF
CD6  CD D0 0E              CALL BALANCE
CD9  D9                    EXX

'DEBIT','CREDIT' OR 'INDEX'
CDA  11 90 0B              DE=0B90
CDD  06 03                 B=3
CDF  CD 34 0F    'DCI 1'   CALL PRINT
CE2  10 FB                 DJNZ'DCI 1'
CE4  CD 3E 00    'DCI 2'   CALL CHIN
CE7  FE 49                 CP=49
CE9  28 8C                 JRZ 'INDEX'
CEB  FE 44                 CP=44
CED  20 06                 JRNZ'DCI 3'
CEF  2E 93                 L=93
CF1  3E 99                 A=99
CF3  18 08                 JR 'DCI 4'
CF5  FE 43       'DCI 3'   CP=43
CF7  20 EB                 JRNZ 'DCI 2'
CF9  2E 9A                 L=9A
CFB  3E 89                 A=89
CFD  32 24 0F    'DCI 4'   (F24) , A
D00  11 66 08              DE=0866
D03  CD 35 0F              CALL PRINT 1
D06  CD AC 0E              CALL FAC

CONTROL
D09  21 10 09              HL=0910
D0C  11 25 09              DE=0925
D0F  0E 40                 C=40
D11  E5          'CT 1'    PUSH HL
D12  D5          'CT 2'    PUSH DE
D13  CD 3E 00    'CT 3'    CALL CHIN
D16  FE 2C                 CP=2C
D18  20 05                 JRNZ 'CON 1'
D1A  E1                    POP HL
D1B  E1                    POP HL
D1C  C3 77 0C              JP 0C77
D1F  FE 1F       'CON 1'   CP=1F
D21  CA C0 0D              JZ 0DC0
D24  FE 1D                 CP=1D
D26  CA A9 0D              JZ 0DA9
D29  FE 2F                 CP=2F
D2B  20 57                 JRNZ ENTRY

END
D2D  EF                    RST 40
D2E  1E
D2F  SWITCH TO REC AND UPDATE LOG
D49  1F
D4A  READY? TYPE YES
D5A  20
D5B  00
D5C  CD 3E 00    'END 1'   CALL CHIN
D5F  CD 3B 01              CALL CRT
D62  FE 53                 CP=53
D64  20 F6                 JRNZ 'END 1'
D66  CD 40 02              CALL CRLF
D69  21 85 0F              HL=0F85
D6C  22 0C 0C              0C0C , HL
D6F  2E DF                 L=DF
D71  22 0E 0C              0E0C , HL
D74  CD D1 03              CALL DUMP
D77  EF                    RST 40
D78  1E                    CLEAR CRT
D79  DONE                  TEXT
D7D  1F                    SCROLL
D7E  BYE                   TEXT
D81  1F                    SCROLL
D82  00                    RTN
D83  76                    HALT

ENTRY
D84  FE 3A                 CP=3A
D86  38 04                 JRNC 'ENT 1'
D88  77                    (HL) , A
D89  23                    INC HL
D8A  18 87                 JR 'CT 3'
D8C  E1          'ENT 1'   POP HL
D8D  E5                    PUSH HL
D8E  13                    INC DE
D8F  F5                    PUSH AF
D90  06 03                 B=3
D92  1A          'ENT 2'   A , (DE)
D93  77                    (HL) , A
D94  23                    INC HL
D95  13                    INC DE
D96  10 FA                 DJNZ 'ENT 2'
D98  3E 2E                 A=2E
D9A  12                    (DE) , A
D9B  13                    INC DE
D9C  1A                    A , (DE)
D9D  77                    (HL) , A
D9E  23                    INC HL
D9F  23                    INC HL
DA0  13                    INC DE
DA1  1A                    A , (DE)
DA2  77                    (HL) , A
DA3  F1                    POP AF
DA4  12                    (DE) , A
DA5  D1                    POP DE
DA6  C3 12 0D              JP 'CT 2'
```

## BACKSPACE

```
DA9 D1       'B/S'    POP DE
DAA E1                POP HL
DAB E5                PUSH HL
DAC D5                PUSH DE
DAD 06 13             B=13
DAF 3E 20             A=20
DB1 77       'B/S 1'  (HL) , A
DB2 23                INC HL
DB3 10 FC             DJNZ B/S 1
DB5 06 07             B=7
DB7 12       'B/S 2'  (DE) , A
DB8 13                INC DE
DB9 10 FC             DJNZ B/S 2
DBB D1                POP DE
DBC E1                POP HL
DBD C3 11 0D          JP 0D11
```

## TOTAL

```
DC0 D1                POP DE
DC1 E1                POP HL
DC2 D5                PUSH DE
DC3 09                ADD BC
DC4 EB                EX DE/HL
DC5 09                ADD BC
DC6 EB                EX DE/HL
DC7 D9                EXX
DC8 D1                POP DE
DC9 EB                EX DE/HL
DCA D5                PUSH DE
DCB 7D                A , L
DCC C6 06             ADD 06
DCE 6F                L , A
DCF 06 02             B=2
DD1 CD 19 0F          CALL SUM
DD4 2B                DEC HL
DD5 06 04             B=4
DD7 CD 1A 0F          CALL SUM 1
DDA 7D                A , L
DDB C6 0A             ADD 0A
DDD 6F                L , A
DDE EB                EX DE/HL
DDF E1                POP HL
DE0 CD D0 0E          CALL BALANCE
DE3 D9                EXX
DE4 C3 11 0D          JP 0D11
```

## DECIMAL POINT

```
DE7 1B       'DP'     DEC DE
DE8 3E 30             A=30
DEA 12                (DE) , A
DEB 13                INC DE
DEC 3E 2E    'DP 1'   A=2E
DED 12                (DE) , A
DEE C9                RTN
```

## REFLECT

```
DF0 7E       'REF'    A , (HL)
DF1 C6 30             ADD 30
DF3 12                (DE) , A
DF4 2B                DEC HL
DF5 13       'REF 1'  INC DE
DF6 10 F8             DJNZ REF
DF8 C9                RTN
```

## MESSAGES (Note that @ signifies the end of string, i.e. 00)

```
E00  * LEDGER *@
E0B  INSURANCE@
E15  CLOTHES@
E1D  HOUSE@
E23  DOMESTIC@
E2C  VEHICLE@
E34  PHONE@
E3A  FEES@
E3F  GIFTS@
E45  A/L@
E49  T.V@
E4D  MEDICAL@
E55  WATER RATE@
E60  SAVINGS@
E68  @
E69  Enter req'd account@
E7D   ACCOUNT@
E86  ITEM@
E8B  BALANCE@
E93  Debit@
E99   Credit@
EA1   or Index?@
EAC  EF(hex)
EAD   Enter , for index / for finished@
ECF  C9(hex)
```

## BALANCE

```
ED0 E5                PUSH HL
ED1 7D       'B1'     A , L
ED2 C6 05             ADD 05
ED4 6F                L , A
ED5 7E                A , (HL)
ED6 FE 09             CP=9
ED8 20 1F             JRNZ 'B3'
EDA E1                POP HL
EDB E5                PUSH HL
EDC D5                PUSH DE
EDD 06 06             B=06
EDF 3E 2D             A=2D
EE1 12                (DE) , A
EE2 EB                EX DE/HL
EE3 21 00 09          HL=0900
EE6 E5                PUSH HL
EE7 3E FA    'B2'     A=FA
EE9 EB                EX DE/HL
EEA 9E                SUB (HL)
EEB 27                DAA
EEC EB                EX DE/HL
```

```
EED  36 00                (HL)=00
EEF  ED 6F                RLD
EF1  23                   INC HL
EF2  13                   INC DE
EF3  10 F2                DJNZ 'B2'
EF5  E1                   POP HL
EF6  D1                   POP DE
EF7  18 D8                JR 'B1'
EF9  06 04     'B3'       B=4
EFB  7E        'B4'       A , (HL)
EFC  FE 00                CP=0
EFE  20 0F                JRNZ 'B5'
F00  2B                   DEC HL
F01  13                   INC DE
F02  10 F7                DJNZ 'B4'
F04  00                   NOP
F05  CD E7 0D             CALL DP
F08  06 03     'B7'       B=3
F0A  CD F5 0D             CALL REFLECT
F0D  18 08                JR 'B6'
F0F  CD F0 0D  'B5'       CALL REFLECT
F12  CD EC 0D             CALL DP 1
F15  18 F1                JR 'B7'
F17  E1        'B6'       POP HL
F18  C9                   RTN
```

SUM

```
F19  B7        'SUM'      OR A
F1A  1A        'SUM 1'    A , (DE)
F1B  F5                   PUSH AF
F1C  7E                   A , (HL)
F1D  D6 30                SUB 30
F1F  30 01                JRNC SUM 2
F21  AF                   XOR A
F22  4F        'SUM 2'    C , A
F23  F1                   POP AF
F24  xx                   ADC/SBC
F25  27                   DAA
F26  EB                   EX HL/DE
F27  36 00                (HL)=0
F29  ED 6F                RLD
F2B  28 01                JRZ SUM 3
F2D  37                   SCF
F2E  EB        'SUM 3'    EX DE/HL
F2F  13                   INC DE
F30  2B                   DEC HL
F31  10 E7                DJNZ SUM 1
F33  C9                   RTN
```

PRINT

```
F34  23        'PRINT'    INC HL
F35  7E        'PRINT 1'  A , (HL)
F36  FE 00                CP=0
F38  C8                   RTZ
F39  12                   (DE) , A
F3A  13                   INC DE
F3B  18 F7                JR PRINT
```

TABLE

```
F41  BD 00 8C 9A
F45  00 AF B6 93
F49  85 00 00 00
F4D  CB 00 00 A8
F51  00 00 D9 C4
F55  00 A1 D2 00
F59  00 00
```

LINE

```
F5B  CD 3C 02  'LINE'     CALL SPACE
F5E  06 2D     'LINE 1'   B=2D
F60  3E 3D                A=3D
F62  CD 3B 01             CALL CRT
F65  10 FB                DJNZ LINE 1
F67  C9                   RTN
```

GRID

```
F68  3E 6C     'GRID'     A=6C
F6A  1E 8B                E=8B
F6C  12                   (DE) , A
F6D  13 A3                E=A3
F6F  12                   (DE) , A
F70  1E AD                E=AD
F72  12                   (DE) , A
F73  1E B7                E=B7
F75  12                   (DE) , A
F76  CD 40 02  'GRID 1'   CALL CRLF
F79  10 ED                JRNZ GRID
F7B  C9                   RTN
```

END OF PROGRAM LISTING

REGISTERS (Note: The first instruction is a title reference)

```
F85  0B 00 00 00 00 00 00    Insurance
F8C  15 00 00 00 00 00 00    Clothes
F93  1D 00 00 00  00 00 00   House
F9A  23 00 00 00 00 00 00    Domestic
FA1  2C 00 00 00 00 00 00    Vehicle
FA8  34 00 00 00 00 00 00    Phone
FAF  3A 00 00 00 00 00 00    Fees
FB6  3F 00 00 00 00 00 00    Gifts
FBD  45 00 00 00 00 00 00    A/L
FC4  49 00 00 00 00 00 00    T.V
FCB  4D 00 00 00 00 00 00    Medical
FD2  55 00 00 00 00 00 00    Water Rate
FD9  60 00 00 00 00 00 00    Savings
```

NOTE: Instructions C71 and C74–76 are necessary to overcome a monitor feature which dislikes the LOAD subroutine to be used by the user program.
0C50 to 0F84 should be dumped onto tape as the main program. The registers are then dumped in blocks as the routine is used.

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Dear Sir,

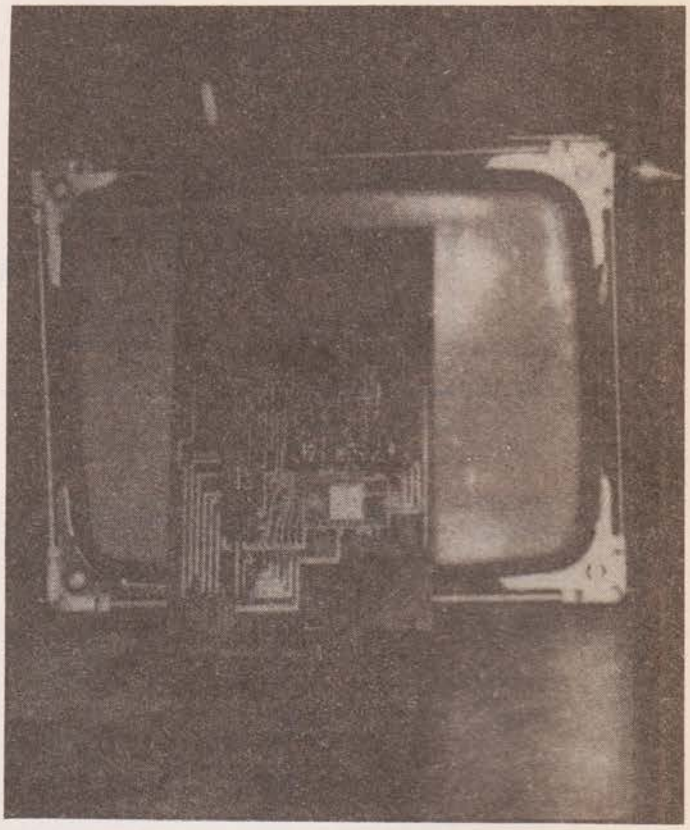
A chance remark to our supplier indicated that an overdue batch of 2708 PROM's were destined to serve as character generators in VDU's brought forth the staggering reply, 'You can't use the 2708 for that job, it will die on you'. I say staggering because we have been doing so – successfully – for some time now and it is most unusual for our supplier, nice chap though he is, to be so knowledgeable. From what he told us, and this has been confirmed by a phone call to the manufacturers, an awful lot of people have wasted time and money nearly building a simple, inexpensive 128 character VDU. I did in fact wonder why the TRITON didn't use one.

The trick is to know what happens inside the chip. The result is that one takes the $V_{DD}$ pin not to +12 V but to VCC instead and then drive its outputs into a conventional 74LS165 circuit. The reduced $V_{DD}$ will compromise the integrity of the 'logic 1' outputs but not enough to worry the 165. The power dissipation within the 2708 will be reduced and the switching speeds will be dramatically improved. One of our VDU's, which has been in service for just over one year, displays a full 1K of characters at 100 frames a second, i.e. nearly 5 MHz.

In the photograph the block above the 2708 is 1K of 8 bit RAM.

Yours faithfully,
John Allen.

Managing Director,
Vanalajohn El, Ltd.



Dear Computing Today,

Yes, all we would be best selling authors would damned well love to have our trembling, anticipatory fingers on a word processor. How infuriating it is to sweat away in an office building by day, where a fortune in computerware lies dormant most of the time, and come home to work on another re–write of chapter four (which started out life as chapter two but the books structure decided otherwise) knowing how desperately useful that equipment could be to little old yours truly!

A micro looks useful from a number of vantage points. Firstly I write 'hard' science fiction and could use a lot of computer time and RAM to build up models of astronomical situations.

But most of all the possibilities for word processing are what look really exciting.

What does a low income creep like me do?

Here I beg for guidance. What I want is something which can handle between 60,000 and 120,000 words of text albeit in chapter sized chunks. The trouble is that I know so little about the hardware and software requirements. I literally don't know what to buy.

The OHIO Superboard II looks nicely economical but how do I know if it will suit what I need? Is it compatible with any particular electric 'golfball' typewriter? And even if it is, which one and how do I lay my hands on the necessary linking equipment?

Yours going mad,
Chris Boyce.

11 Downside Road,
Glasgow G12 9YB

Dear Sir,

I have just finished reading the first issue of Computing Today and I feel I have to say I am rather dissapointed.

I read two other computing magazines and for the same fifty pence I get better quality paper and with it far superior photographs (some in your magazine really are atrocious–the page titled Tangerine Dream was just a page–the majority of which was taken up by a mysterious black square). The argument that money saved on printing is used to produce more articles can't be used since the other publications have as many if not more articles.

Do I detect a slight bias towards the Triton? For the thousands of people who don't own one of these there were nine wasted pages in the first issue (approx 20%). Surely Triton owners could pay and be sent this information independantly and a brief summary appear in the magazine.

I suppose the article on Beginning Basic will have to stay, every other computing magazine has done it. Books such as Illustrating Basic by D.Alcock cannot be bettered for their self teaching of this language (and it costs less than two pounds).

After I've said all this I'm still going to read Computing Today and I hope you find my comments constructive.

Yours faithfully,
Derek Anderson.

46 Hawes Side Lane,
Blackpool,
Lancashire FY4 4AS

*Dear Sir,*

*In the first part of your article, Bits, Bytes and Bauds, there is an error on page 16. The third paragraph states that the two tones normally used by amateurs are 2125 Hz and 2125 Hz +/- 170 or 850 Hz. This statement is not true. The recommended tones are 1445 Hz (mark) and 1275 Hz (space) giving a shift of 170 Hz. The actual tone frequencies are not too important when using a single sideband suppressed carrier, although the shift is. On VHF, the most common mode for transmitting RTTY is frequency modulation where the tone frequencies are required to be accurate. Incidentally the Baud rate now used by amateurs is 45.45 Baud.*

*Whilst you are commended for mentioning some of the techniques employed by amateurs you do not mention the ubiquitous Creed machines. Although these machines might be considered as being suitable only for the scrap heap, a very large number are still in use by amateurs. Although they are relatively slow devices and unable to print all of the characters in the ASCII font, I would have thought that they could still find a home with microprocessor fanatics.*

*A number of amateurs are using microprocessor systems for the transmission and reception of the Baudot code and the software for ASCII/Baudot and Baudot/ASCII conversion is very simple, in fact a very good exercise for the beginner.*

*The two machines I would suggest as being suitable for use with a microprocessor are the Creed 7E/RP teleprinter with tape perforator and the Creed 6S series tape readers. These are widely available on the surplus market for £25 and £10 respectively, a bit different from the asking price for an ASR 33!*

*Perhaps your article could include this information together with the code conversion routines, I believe it would be appreciated by a lot of readers who may not even be aware of the available alternatives.*

*Yours faithfully,*
*M.J.Strange.*

*G8HH0,*
*19 Wilsheres Road,*
*Biggleswade,*
*Bedfordshire SG18 0BU*

---

*Dear Sir,*

*I read in the magazine that you wish to know how people are using microcumputers, and notice that nothing has appeared about their use in secondary education. I have been involved with teaching computing and using computers in Physics teaching for about 8 years, having also tested various Schools council sponsored programs, mainly using a hard copy terminal. We now have a TRS–80 with Level 2 16K and are busy developing a multitude of uses at all ages and subjects, and finding out its capabilities for certain administration work.*

*So far we have about 20 Physics and Biology programs which we are using as a normal part of class teaching, together with a 'House Design' program which 11 and 12 year olds will use in their Art and Design lessons. A simple 'letter writing' word processor is under developement for the commerce department. This is in addition to use in teaching Computer Studies and many more ideas are awaiting time.*

*Several weeks ago a colleague and myself assisted by the County Maths and Science Advisors run a week long course for 35 of the very bright 12 year olds in Cheshire and used computer simulation to compare theoretical predictions with measured data in Electronics and Ecology. We had two TRS–80's and a Centronics printer.*

*Since we don't yet posess a printer all permanent output is photographed on 35mm film (black on white) which can either be read normally, projected or printed. Graphs are copied with tracing paper. This has proved a cheap and accurate idea for our purposes.*

*We intend to expand our computer facility and its use in the school so that pupils and staff accept the use of computing as a valuable teaching aid.*

*A problem with the Computer Studies work is data preperation and one idea we are working on is to have a set of units all connected to one tape punch, since we still find paper tape a convenient medium for short programs. Each unit has a simple keyboard and a 1 or 2K 8 bit store which is large enough to hold most pupil programs. The keyboard is a piece of RS Components stripboard cut and wired so that by wiping a stylus across 10 strips the ASCII code and two control pulses are produced. When program loading is completed it is output to the fast punch. The proto type is now under construction.*

*Yours faithfully,*
*T.J.Cross.*

*Head of Physics,*
*Great Sankey County High School,*
*Barrow Hall Lane,*
*Great Sankey,*
*Warrington WA5 3AA*

---

*Dear Sir,*

*I refer to your excellent March issue and would like to say that I have placed a regular order with my newsagent.*

*I tried the Card Sharp program on my IBM 5110 but was dissapointed to find that it did not work. Either there is a bug in the program or I made a copying mistake that I cannot find. You will see from the enclosed printouts that though all four aces had been used the program called for the suit of (another) ace.*

*Please note that the only ammendments that I made to the program were to input the player's name using variable @$ and a routine to end the program if 'end' is input as an answer. Also I renumbered the program statements to allow further ammendments.*

*Incidentallly I also tried the Stomper program but it does not appear to be suitable for the BASIC used in my machine. Am I right?*

*Yours faithfully,*
*R.K.Prater A.C.I.S.*

*5 Stratford Way,*
*Watford WD1 3DH*

# BEGINNING BASIC

You may remember, if you have been following the series, that we covered the LET statement in part 2. This was the first of several statements that can be used to assign a value to a variable. This month we begin by looking at two more assignment statements.

## INPUT

So far we have only seen the computer acting as an advanced calculator performing great amounts of arithmetic at fantastic speeds, but it can also be used as an interactive device, capable of asking questions and accepting answers. INPUT is the statement in BASIC which allows the computer to accept answers to questions.

Consider the following:—

```
10 PRINT "INPUT AMOUNT (IN POUNDS)"
20 INPUT P
30 V=P+(P*8/100)
40 PRINT "THE VALUE OF V IS",V
50 PRINT
60 PRINT "DO YOU WISH TO INPUT MORE DATA"
70 PRINT "PLEASE TYPE 1 FOR YES OR 0 FOR NO"
80 INPUT A
90 IF A=0 THEN END
100 IF A=1 THEN 10
110 GOTO 70
```

This is a program which will add 8% VAT on to any amount of money that you INPUT in line 20. What happens is this:—

Line 10 is a PRINT statement which is used here to give you an instruction. It is telling you to INPUT the amount that you want the VAT added to. Line 20 is the INPUT statement and when the computer encounters this line it will print a question mark on the screen (as a prompt to tell you that action is required) and then it will stop and wait for you to input a number from the keyboard (say 100) and enter it with a carriage return. When the computer has this value, it will be assigned to the variable which appears after the word INPUT (in our case P) so that when we reach line 30, P has the value 100 that we have just INPUT. Line 30 calculates the VAT and adds it on; line 40 prints the answer; line 50 prints a blank line; then line 60 asks if you wish to go through the process again with a new value of P and line 70 gives you the format you should use to make your reply; line 80 is the second INPUT statement which will take your answer from you and assign the value to the variable A; line 90 ends the program if you answered 0 (no); line 100 branches you back to line 10 if you answered 1 (yes) to begin again, and line 110 branches you back to line 70 to reprint the answer format if your answer was anything other than 0 or 1. The flow chart for this program would appear as in figure 1.

It is possible to assign values to more than 1 variable in a single INPUT statement. The format of the INPUT statement would then be as follows:—

```
100 INPUT P,Q,R,S
```

with each of these variable names separated by a comma. One thing to note, however, is that when you answer such an INPUT statement, you must enter as many numbers as there are variables requiring values, and each number you enter must be separated by a comma, so that:—

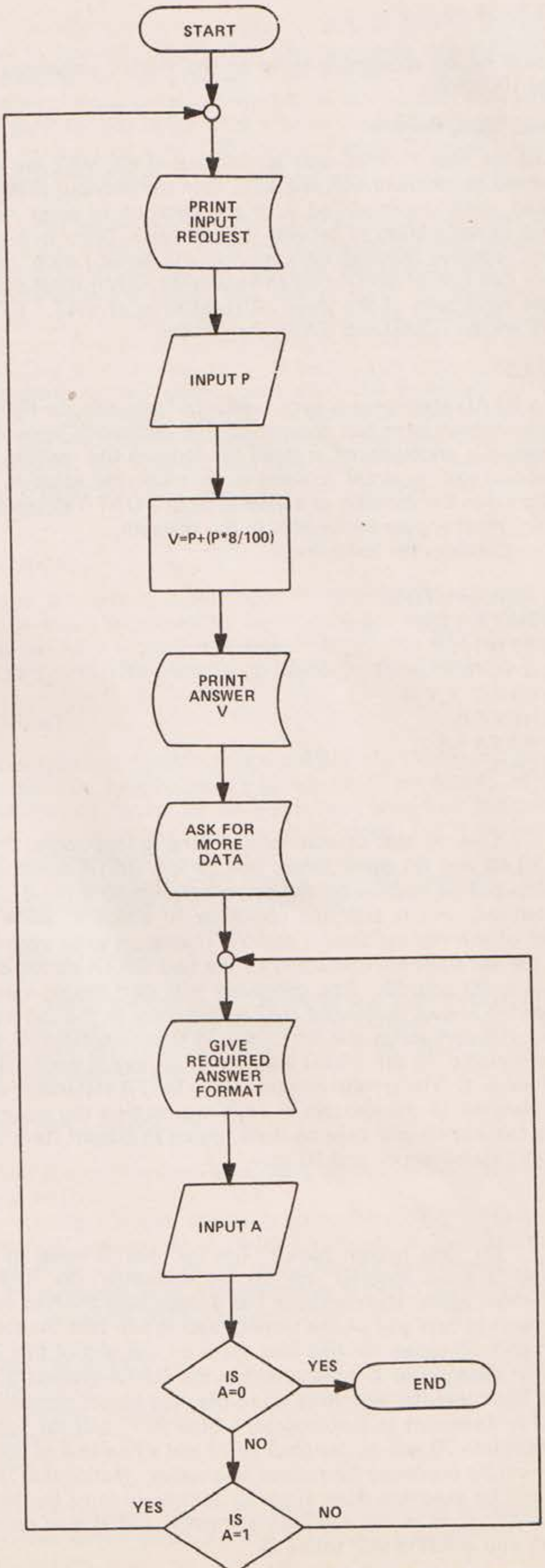



Fig1. Program Flowchart.

10,20,30,40

would be an acceptable reply to the INPUT statement on line 100 above.

**Read, Data, Restore**

Suppose now that as well as calculating 8% VAT we also wanted to calculate 10% and 12%, then the previous program could easily be modified with the addition of some more lines of calculation to provide the answers. There is, how–ever, another method of achieving the same result, using only one line of calculation and going through it three times, once with each of the three different rates of VAT. To do this, we use READ and DATA statements.

**READ**

The READ statement is very similar in format to the INPUT statement we have just considered, the difference being that when it is encountered, instead of stopping and waiting for the operator to enter a number, it takes the value to be assigned to the variable or variables from a DATA statement, which must appear somewhere in the program.

Consider the following:–

```
10 FOR B=1 TO 3
20 DATA 1,2,3
30 READ X,Y
40 R=X*Y
50 PRINT X,Y,R
60 NEXT B
70 DATA 5,6,7,
80 END
```

Line 10 tells us that we are going to loop round lines 20,30,40 and 50 three times: line 20 is a DATA statement which will be ignored by the computer; line 30 is the READ statement, and it tells the computer to assign a value to each of the two variables X and Y. The values to be assigned to the variables are contained to the two DATA statements in lines 20 and 70. The computer will start taking values from the lowest numbered DATA statement in the program (line 20) and assign the first value in that statement to the first variable in the READ statement, so here X would take the value 1. The second number in the DATA statement will be assigned to the variable Y, so Y would take the value 2. The calculation will then be done, giving an output from the PRINT statement on line 50 of:–

```
1         2         2
```

We then branch back to line 20 (with B equal to 2) which is again ignored, and so we encounter the READ statement again. The computer has already used the first two numbers of data and on the second reading will take the sec–ond pair of values (in this case the 3 on the end of line 20 will be assigned to X which finishes the DATA statement so that the computer will move up to the next higher numbered DATA statement in the program – line 70 – and the value 5 from line 70 will be assigned to Y) and a new line of out–put will be produced from these two values. Notice that line 30 will be executed three times so that there must be three pairs of values in the DATA statements, and if you count them you will find that this is so.

As you may have gathered from the dub–heading, the READ, DATA statement has one other facility – RESTORE.

If you imagine a pointer, stored in memory, to "remind" the computer which is the next piece of DATA to be READ, then the effect of the RESTORE statement is to return this pointer to the first piece of DATA in the lowest numbered DATA statement. The simple program below (infinite loop) gives an example of its use.

```
5 INPUT A
10 FOR B=1 TO 3
12 READ C
16 PRINT A+(A*C/100)
20 NEXT B
30 PRINT
35 RESTORE
40 GOTO 5
60 DATA 8,10,12
80 END
```

Here, for each value of A input in line 5, we add on VAT using three different VAT rates, 8%, 10% and 12%.

A sample running of the program could look some–thing like this:–

```
?100
108         110         112
?150
162         165         168
?
```

etc. I'll leave you to work out the details (good practice).

**GOSUB Return**

GOSUB is the statement used in BASIC to branch to a sub–routine. The general format of this instruction is:–

```
10 GOSUB xxx
```

where xxx is the first line number of the sub–routine. A sub–routine would normally be used where a particular set of calculations or operations occur several times in a program, and this would save having to write out the whole operation every time it was to be used. The GOSUB in–struction is very similar to the GOTO statement, except that before the branch is made, the line number containing the GOSUB statement is stored. After the computer has executed the sub–routine, we make it encounter a RETURN statement. At this point, the computer retrieves the line number of the GOSUB instruction which called the sub–routine, and branches control back to that point. The program then continues as normal.

Consider the following example:–

```
5 PRINT "INPUT CIRCLE RADIUS"
10 INPUT R
20 D=R*R
30 GOSUB 500
40 PRINT "AREA IS",Q
50 D=2*R
60 GOSUB 500
70 PRINT "CIRCUMFERENCE IS",Q
80 END
500 Q=D*3.14159
510 RETURN
999 END
```

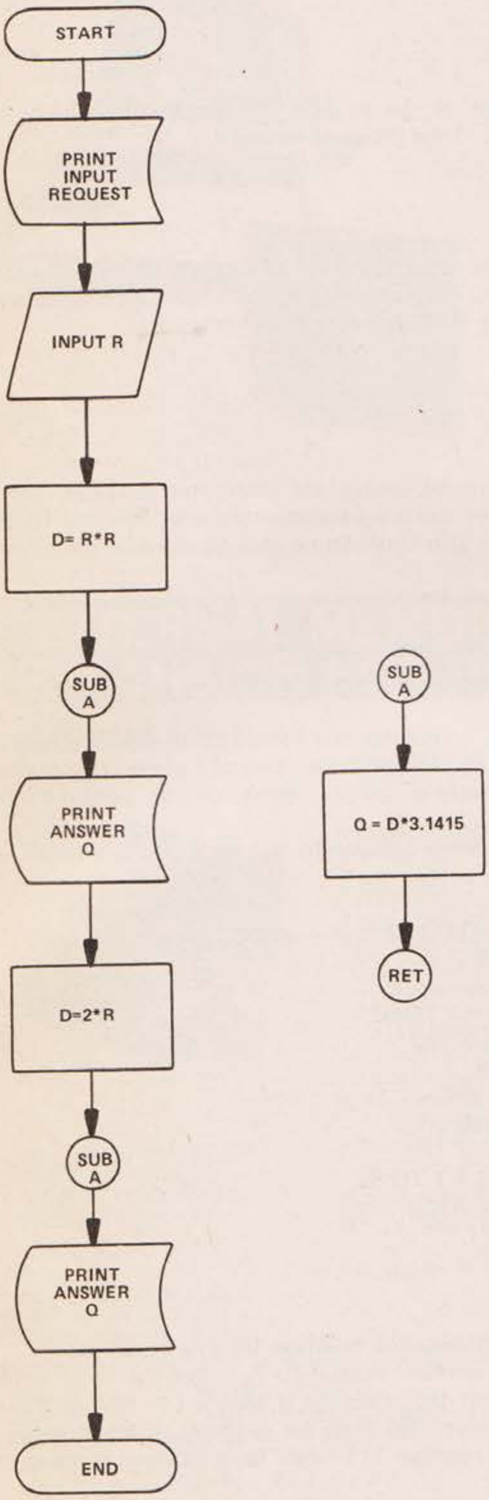



Fig 2. Circumference program flowchart.

Notice that there are two GOSUB 500 instructions (one in line 30, one in line 60), but only one RETURN instruction in this program. As explained earlier, this is because the computer has stored the line number containing the GOSUB instruction so that when the RETURN instruction is executed (line 510) the computer "knows" which GOSUB instruction to RETURN to.

The sub–routine in the above example is only multiplying by $\pi$ and then returning control to the main program. Lines 5 to 40 use the sub–routine to calculate the area of a circle from the radius you INPUT (line 10) and lines 50 to 70 use the sub–routine to calculate the circle's circumference. One further point to note is the inclusion of line 80. This is most important. If we did not include an END statement at this point, then after the execution of the PRINT statement in line 70, the computer would crash into the sub–routine by executing line 500, and then would bomb–out trying to execute line 510, as it has no RETURN line number stored. (See fig. 2 for the flow chart of this program.)

**Functions**

There are very few functions in tiny BASIC (we will see many more when we go on to consider extended BASIC) and we have already met one of them, the RND function, in part three. We will now go to look at three more.

**TAB(X)**

This function is used in the PRINT statement and is very useful for spacing out headings and generating vertical columns of figures (if we want more than four columns so that we could not use the print zones). It is also useful for plotting graphs.

If you have ever used a standard typewriter, then you should know all about TABS, eg –

```
20 PRINT TAB(5),"*"
```

When the computer comes to deal with this statement, it will output 5 spaces (5 being the number in the brackets following the TAB). Following this, it will print the asterisk. If the statement had been –

```
20 PRINT TAB(8),"*"
```

then 8 spaces would have been output before the asterisk, and so forth.

The number in the brackets of a TAB function can also be replaced by a variable name or any expression, in which case the computer will TAB out to the correct value of the variable or expression before printing anything else.

Consider the following:–

```
10 FOR X=1T05
20 Y=X*X
30 PRINT TAB(Y),"*"
40 NEXT X
50 END
```

You will find, if you work through this program, that it will print a graph of $Y=X^2$ (rotated clockwise 90°). Try it, and see.

One last point about TAB is that the comma which follows is not interpreted by the computer as an instruction to move into the next print zone, but merely to separate the TAB function from anything which follows it.

**ABS(X)**

This function produces the absolute value (or modules) of the contents of the brackets (numbers, variables or express–ions) which means that whatever sign (positive or negative) the contents of the brackets have now, the sign will be positive when the ABS function has been performed, so that–

```
10 X=ABS(T+3)
```

would have the value of +1 if T was –4, or the value of +4 if T was +1, etc.

**INT(X)**

This function is not applicable to computers operating with integer – only arithmetic for reasons that will become obvious in a moment. The brackets after the INT function can contain a number, variable or expression, and what the INT function does is to return the largest integer which is less than or equal to the contents of the brackets. This may sound something of a mouthful, but what it really means is that it makes positive numbers less positive, and negative numbers more negative.

For example:–

X would take the value 2 if we executed:

```
10 X=INT(2.9)
```

and X would take the value –3 if we executed:

```
10 X=INT(–2.9)
```

There is one other statement that we need to con–sider in tiny BASIC before we go on to look at commands.

**STOP**

The STOP statement is similar in effect to the END state–ment, in that execution of the program ceases, but when a STOP statement is executed it also generates a print out, usually something like this:–

```
BREAK AT xxx
```

where xxx is the number of the line which contained the STOP statement. This can be useful to "freeze" the display of a large table, for example, because one other facility of the STOP statement is the ability to start the program up again from the point at which it left off. To do this, we use the first of the commands.

**CONT**

This command is short for CONTinue, and is used to re–start a program whose execution has been halted by means of the STOP statement considered above.

**RUN**

This is the command which is used in BASIC to cause execution of a program in memory to begin. Most com-puters will also accept RUN command in the following format:–

```
RUN xxx
```

where xxx id the number of the line at which you wish execution of the program to begin.

**NEW**

This is the command in BASIC which tells the computer to erase the current program from memory to create memory space for a NEW program or other work.

**LIST**

This command causes the computer to LIST the current contents of the program memory and, like the RUN state–ment, it is also usual to be able to execute the command:–

```
LIST xxx
```

where xxx is again the line number of the first line to be listed.

This completes our look at tiny BASIC. Next month we go on to look at the writing of a game program for a tiny BASIC machine before going on to consider extended BASIC.

A sample answer to last month's homework is given below.

```
10 FOR A=1TO 52
20 A(A)=A
30 NEXT A
60 FOR B = 1 TO 52
70 R = RND 52
80 X = A(R)
90 A(R) = A(B)
100 A(B) =X
110 NEXT B
120 FOR C = 1 TO 52
130 PRINT A(C);
140 NEXT C
150 PRINT
160 END
```

The homework question for this month is:–
Given any number from 0 to 7, convert it to a 3–bit binary number such that each bit is assigned to one of three diff–erent variables. So that, for example, if the number was 7, the binary number 111 might have its three digits as follows:

```
H = 1
J = 1
K = 1
```

so that if we were to execute the statement PRINT H,J,K then the output would be the binary number.

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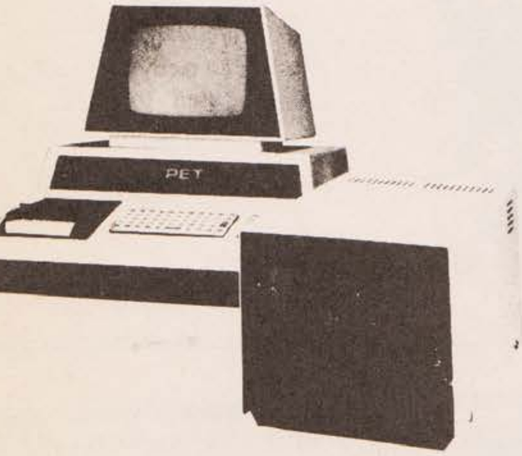


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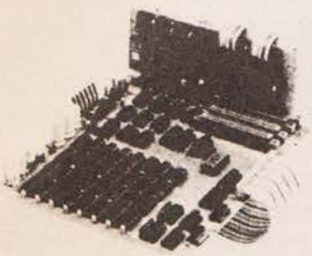

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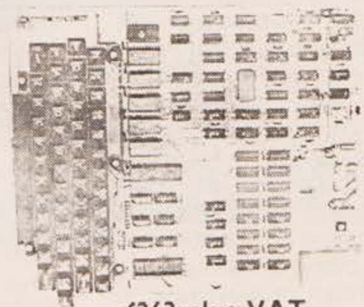

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A SOFTWARE CONTROLLED VDU (SCVDU) (otherwise known as a memory-mapped VDU) is one in which the memory that is storing the VDU's display is part of the processor's normal main memory. Hence the processor can read or write directly to any location on the screen without having to progress sequentially down the screen as in conventional VDUs.

The advantages of the SCVDU are almost limitless and new applications will keep occuring to you as you use one. For example, the processor can write to this memory as quickly as it can write to any other memory, so a complete screen of information can be output quicker than you can blink. This allows you to continually look at listings of a program as you modify it without waiting hours. If the screen is displaying the output of a game the display can be updated every few milliseconds to provide the effect of movement. It is possible also to just update one portion of the screen and leave the rest static, such as having a time count in one corner of the screen or having a 'Bytes left to load' count when reading from tape. (This is one facility I wouldn't be without.)

Any portion of the screen can be scrolled as desired, maybe three lines scrolling at the bottom with the rest of the page staying fixed, or scroll downwards just for variety. Writing across the screen and down gets dull, why not make the processor write vertically for a change? Because the processor can read back from the screen it is possible to do text editing on the screen including insertion and deletion and then simply read it back without the need to keep a scratch copy elsewhere.

Let your imagination run wild, the display possibilities keep coming.

## Screen Format

The characters are displayed as 64 characters per line and 16 lines on the screen. The character generator displays a 7 x 9 dot matrix with appropriate lower case characters (g, j, p etc) descending below the line by 3 dots effectively giving a 7 x 12 display. The font has 128 characters including upper and lower case letters and various mathematical and general symbols
Other fonts are also available, in pin compatible ROMs, such as Greek, French, German and Japanese letters.

## Flashing Characters

With a SCVDU the processor can make a character(s) flash by writing the character then a blank after a suitable delay and then repeating this cycle. However, this keeps the processor busy when it could be away doing better things and the flash rate will vary depending on how much other work the processor is doing at the time. A much neater alternative is to have the flashing done in hardware and selected by a bit (bit 8) with each character which is how this VDU approaches it. Thus any character on the screen can be selected as flashing or not. The flash rate is set with a preset control on the board.

## Black on White Characters

The area around a character is turned white and the character is seen as a black letter in this area. This is particularly useful to indicate a cursor as it can be backspaced over characters leaving the characters readable. The inverse video function can also be used to emphasize a line. As with the flashing function, Black on White is selected by an extra bit for each character. (Bit 7).

## Chunky Graphics

These are low resolution graphics that are useful for large headings or borders, or for simple diagrams. The graphics are formed by taking the area occupied by one character (the same area seen as white around a Black on White character) and breaking it up, two across and four down. (See How it Works). These eight dots can be selected as White or Black by the eight bits that are stored for the character that would have occupied the space. Graphics or normal is selected by another bit for each character.

## Memory Organisation

As you can see from the above points, there are quite a few bits stored for each character, ten in fact. This is how they are organised:

| | |
|---|---|
| Bits 0-6 | Seven bit ASCII code (giving 128 characters) |
| Bit 7 | Black on white bit |
| Bit 8 | Flashing bit |
| Bit 9 | Graphics bit |

Storing 10 bits per character presents a problem for an eight bit microprocessor. The way around the problem is to store the first eight bits of information for the 1024 characters on the screen as one kilobyte and then store the extra two bits exactly 1024 addresses above the character that they belong to. Thus the VDU occupies 2 Kilobytes of addresses but the second K only has two bits.

As an example of the above arrangements, if you locate the VDU at F000 HEX then it will occupy from F000-F7FF (2K). The character in the top left hand corner of the screen will be stored at F000 HEX and the bits to make this character flash or be a graphic are stored at F400 HEX. The last character (at the bottom right hand corner) will be stored at F3FF HEX.

### S100 Bus Standard

The S100 standard is a 100 pin bus standard that was introduced by Altair and has been widely accepted in the USA. S100 was originally designed around the 8080 processor but can be adapted to virtually any processor. If your system is not S100 oriented all you need do is plug the VDU into a 100 pin socket and wire the appropriate signals out of your processor. None of the signals used are specialised and should be available on any processor or at least derivable with two or three gates.

In order to minimise both the size and complexity of the circuit diagram, the two blocks of RAM have been represented as one box on the drawing. On the top edge of the box, it can be seen that each DO line goes, via a buffer, to pin 11 of a different 2102 RAM IC, and likewise, each of the DI lines comes from pin 12 of a different IC (right edge). The address lines go to all of the IC's in parallel. Note also that, in S100 parlance, the DO (Data Out) lines are outputs from the CPU (hence inputs to the VDU) and the DI (Data In) lines are CPU inputs, (hence outputs from the VDU).

$\overline{\text{MERQ}}$ (pin 65) is not a regular S100 signal, but was included on the prototype as a means of avoiding some potential problems with the VDU responding to 'mirrored' I/O addresses put out on the upper eight bits of the 8080 address bus. In practice, this is not a

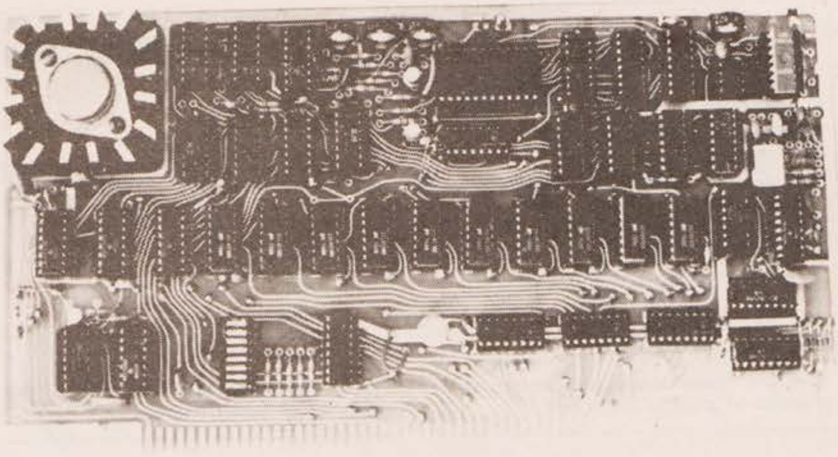


Fig 1. The VDU board.

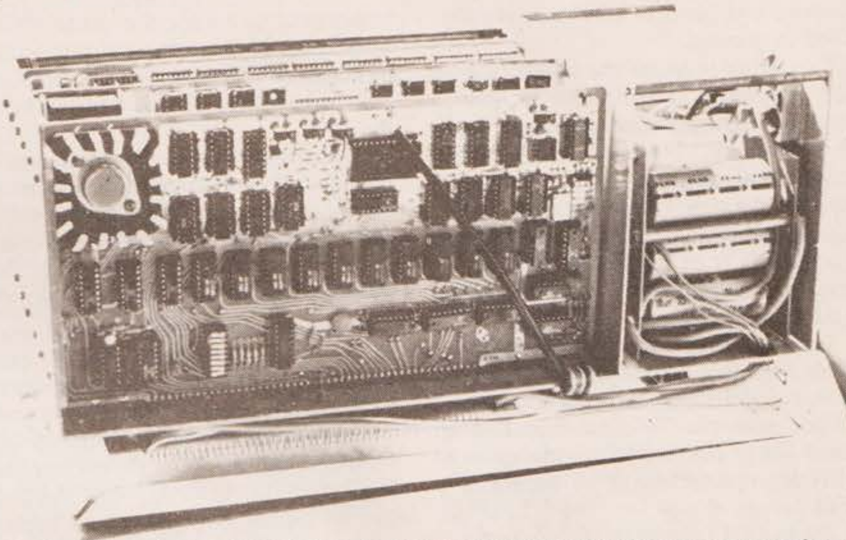


Fig 2. The VDU is designed to plug into any S100 microcomputer system as is shown here.

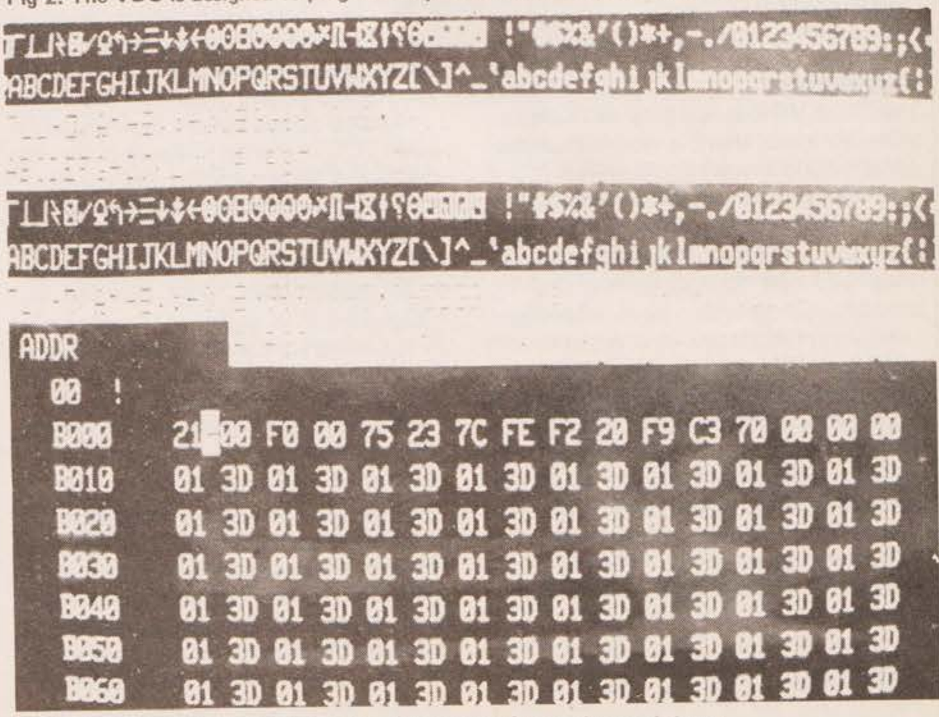



Fig 3. This photograph is taken from the screen of a monitor and shows the character set of the VDU.

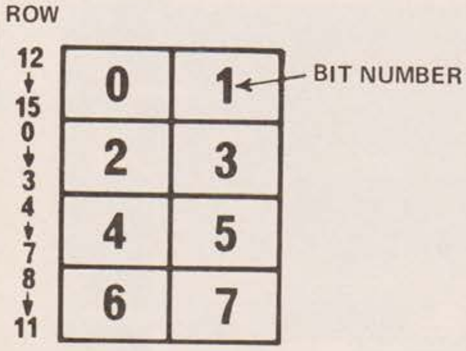



**Fig 4. Each character space is broken up for the creation of graphic characters.**

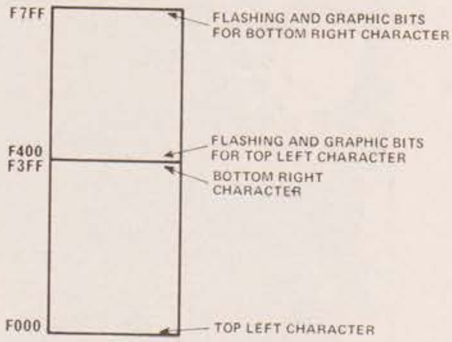



**Fig 5. The VDU actually looks to the processor like 2K of memory.**

problem, and pin 7 of IC34 is normally linked to ground.

Two other links on the board (above IC39 and above IC10) allow 32 character/line operation and operation with a 6 MHz clock. However, the 6 MHz clock modification is not fully implemented, being a 'hangover' from a previous prototype design - nonetheless, we have left it in for the benefit of those incorrigible individuals who must modify their projects.

The data sheet for the MCM6574 reveals that this device requires +5V, +12V and -3V supplies. Where, I hear you ask, does the -3V come from? The answer lies in IC9, a 7404, three gates of which are connected as an oscillator which pumps charge into the D12-D15, C9, 10 and C17 network to produce a negative supply.

## Construction

The S100 VDU is not very difficult to assemble since there is no mechanical construction involved. However, it is a very complex board, and several points should be noted in order to ease construction. Firstly, the board was designed to be through-hole plated to simplify construction and improve reliability. Although it is possible to build the VDU on a double sided board by soldering links through the board, we strongly recommend use of the through-hole-plated board. Our prototypes were constructed the hard way, by soldering both sides of the board, and believe me, it's no fun! Although the through-hole-plated board is more expensive, we believe the extra money is well worth spending.

If you are using your own printed circuit board, you should start by soldering links through the board in positions which will later be covered by IC's —i.e. IC4, IC11 and IC16. It is virtually impossible to solder the other links in until most of the other components are in place, so these will have to wait until later, when they can be inserted before the IC's.

Construction should commence with the insertion and soldering of all IC sockets (if used), SW1 and the links. Care should be taken with the orientation of sockets, and later, IC's, since they are not all the same way up. All the resistors should be inserted next, followed by capacitors C1-C28, except for C13 which is later mounted on the back of the board. The diodes and transistors can now be soldered in, followed by the potentiometers, and IC42 with its heatsink. Now the board can be flipped over, and C13 soldered onto the back of the board, followed by C29-C39. These 10 nF bypass capacitors mount on the back of the board, across the supply pins of IC's 2, 3, 5, 6, 9, 11, 12, 15, 16, 17 and 18.

At this point, before inserting any other IC's, it is wise to apply power to the board and check for the correct voltage at the regulator output and also on pin 3 of IC4 (which is not yet inserted). If these points are at +5V and +12V respectively, then proceed to either plug in or solder in the remaining IC's, taking care with orientation, and finally solder the crystal in, being careful not to apply excess heat.

This concludes construction of the VDU, and all you have to do now is work up the courage to switch on!

Although it would be possible to assemble this project and have it work first off, the number of components and solder joints and the tendencies of Mr Murphy (and his famous law) make it quite probable that something won't be right, unless you are extra careful. So with this in mind we have outlined a logical procedure for debugging the VDU.

# HOW IT

### Synchronising Pulse Generator

The start of the chain is the 12MHz crystal oscillator (IC9) which is divided down to 15,625 Hz and 50 Hz (by IC's 38, 39, and 40). The 15,625 Hz signal triggers a 5 $\mu S$ monostable (IC 41A) to provide line synchronising pulses and the 50 Hz signal triggers a 300 $\mu S$ mono (IC41B) for field synchronising pulses. These synchronising pulses are added to the final video signal before it leaves the board to give composite video out as well as providing a timing reference for the rest of the VDU.

### Character Generation

It is not intended to give a complete explanation of how characters are generated on a screen as this has been explained in previous VDU articles and the basic principles used here are the same. The characters are displayed on a matrix 7 dots across by 9 high. The character generator ROM (IC4, MCM6574) outputs the 7 bits across each character in parallel as it is told what character is being constructed (on pins 15, 16, 12, 11, 9, 8, 4,) in ASCII code and which row of the character is selected (on pins 21, 22, 23, 24).

IC 5 and IC 6 are Quad 2 in 1 out multiplexers which simply act as an eight pole two position switch. They connect the output of the character generator ROM (IC4) or the output of the graphics multiplexer (IC14) through to the parallel inputs of the 8 bit shift register (SR) (IC7). Ignoring the graphics mode for a moment, the output of the ROM is connected through to the SR and the eighth bit is tied low (pin 14, IC5) to give black; this is the space between each character. Once the SR is loaded with this information and is clocking it out at the right rate (12 MHz) the RAMs and ROM are already looking up the information for the next character as both the RAMs and the ROM have a noticeable access time to consider.

The data out of the SR is essentially the information that goes to the screen, although there is some gating after it to invert the data for flashing characters and inverse video, as well as blanking circuitry which will be discussed later.

### Counters

The above combination of RAM, ROM and SR will happily produce characters all over the screen provided the RAMs are given information about which character is being produced (ie character on the line, and line on the screen) and the ROM is told which row of the character is being produced, so there are three sets of counters which keep track of this information. The first set (ICs 11 and 12) count 0-63 for character on the line (COL). This counter is incremented by the same pulse that loads the SR (from IC13, pin11) at the end of each character. When this set of

# WORKS

counters reaches zero (64) it sets the first 'end of line' flip flop (IC2B). IC2B enables the second 'end of line' flip flop to set after the 64th character has been clocked out by the SR. This combination of two flip flops is necessary to provide a one character delay, otherwise the screen would be blanked as soon as the counters reached zero and the 64th character would be lost. Aha! When the second 'end of line' FF has set it inhibits any further clocking of the SR and COL counters and forces the screen to black (via the diode to IC16, pin12) until the beginning of the next line. The clearing of the next FFs is discussed under 'Positioning'.

The second counter that counts the row of the character (IC15) is incremented every time the 'end of line' FF sets. One of the confusing parts of the circuit is the fact that this counter actually counts 12, 13, 14, 15, 0, 1, 2, . . . . . 10, 11 for each character. The ROM outputs blanks for rows 12, 13, 14, 15 so this puts the four lines of blanks above the character instead of below. The result of this is that each character is centred in the character position for Black on White characters, rather than being hard up against the top of the white area. The effect of the row counter counting in this sequence is achieved by incrementing the third counter (the 'line on screen', LOS) when the row counter reaches 12. (IC 16 pins9, 10 gates C, D of Row Counter).

The LOS counter counts 0-15 for the 16 lines of characters on the screen and when it overflows to zero it sets the 'end of page' flip flop (IC2A). This will occur at the end of a line, as that is when the row counter is incremented, that then increments the LOS counter, so the 'end of line' flip flops will both be set. The end of the page' flip flop simply stops the 'end of line' FFs being cleared until the top of the next page.

### Positioning

The position of the characters on the screen is determined by the time after the synchronising pulses that the EOL and EOP FFs are cleared. These two times (Vertical and Horizontal) are set by two monostables (IC3A and IC3B respectively) which are triggered off the leading edges of the vertical and horizontal synchronising pulses respectively. As each of these monos drop off they cause a negative going pulse via a capacitor to the reset pins of the appropriate FF. The EOP FF holds a reset on the horizontal positioning mono.

The final counter which wasn't mentioned earlier is the counter (IC 13) which counts the number of bits that the SR has clocked out to provide a load pulse for the next character. This counter is clocked at the same rate as the SR (12 MHz) and counts to 9 before resetting to zero, so the SR clocks out the eight bits

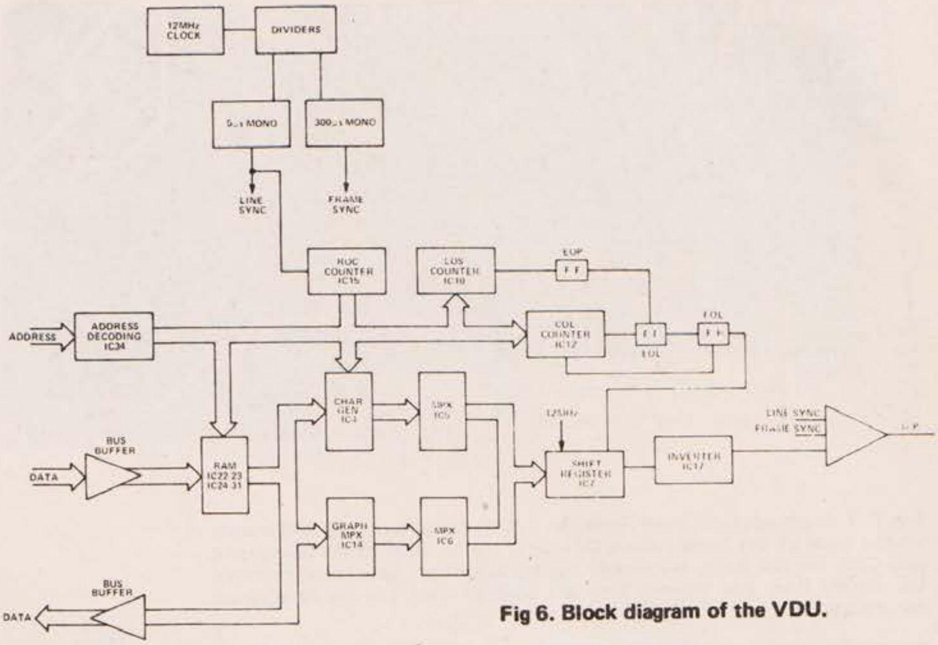



**Fig 6. Block diagram of the VDU.**

it has been loaded with plus one more which will be whattever was on the Serial In Pin of the SR (pin 10) when it clocked out the first bit. This is arranged to be a zero (black) when making characters or whatever is appropriate when making graphics.

### Graphics

The graphics circuitry only needs to be told which row of the line is being made to select which two bits to feed to the SR (via the graphics/character multiplexers). The same two bits are selected for four rows so only the two highest bits of the row counter are used by the graphics multiplexers (IC 14).

### Black on White Characters (Inverse Video)

The 'black on white' (BOW) bit (bit 7) is latched by a 'D' Flip Flop (IC 18a) at the same time the SR is loaded. This bit is forced to normal when a graphic is being made, (IC16A) as there is obviously no point in inverting a graphic and the eighth bit (bit 7) is used by the graphic anyway. The output of the FF controls an exclusive OR gate which acts as a switchable inverter, if a '1' is held on the 'control' input (pin 10) the data on the other pin will be inverted at the output.

The XOR is in the output of the SR so when it is switched to the invert mode it simply inverts the bit stream.

### Flashing

The flashing bit (bit 8 – 1st bit 2nd K) is latched in a 'D' FF (IC 18B) the same as the BOW bit described above. When a '1' is stored in the FF it forces the output to black. The flashing is generated by an oscillator (IC8) clearing the FF down at the flash rate.

### On The Bus Side Of The Board

To the processor, the VDU looks just like normal memory with the exception that the upper 1 Kilobyte only has 2 bits. Thus the circuitry involved here is fairly typical of any memory board, the noteable difference is that the lower 10 address bits to the RAMs go via multiplexers so that the VDU counters can scan the RAMs when the processor is not accessing them.

The incoming data (off the bus) is buffered by IC35 and part of IC37 before going to the RAMs. The outgoing data is buffered by IC36 and IC37 which are enabled whenever the board is addressed for a read cycle.

IC34 is a comparator that looks for a match between the DIP switches and the high order address bits on the bus. When it finds a match (pin 9 = '0') it means the board is being addressed and the RAMs are taken away from the VDU temporarily. During this period the screen is forced to black (by the transistor off IC34's output otherwise a series of white flickers would be seen on the screen.

### Output Circuit

The output circuit combines the digital (5 V) signal representing the black and white information with the vertical and horizontal synchronising signals to give an analogue video signal which is the output signal from the VDU board. The shift register is being clocked at 12 MHz, so the worst case output signal would be one bit on and one bit off which represents a 6 MHz video signal. The transistor used in the output stage is critical as it needs a very fast rise time. A domestic TV receiver has a sound trap at 5 MHz after the IF strip so the loss of quality by modulating the VDU signal would be considerable. For this reason it is suggested that the TV set be modified to accept video in or a proper video monitor be used. A lot of sets on the market today have video in and out facilities for VTR's already fitted.

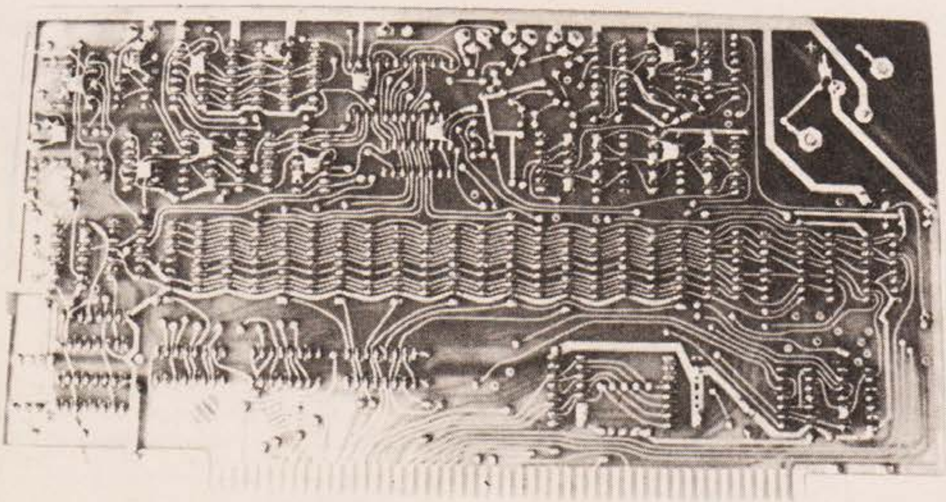


**Fig 7. This photograph shows how the bypass capacitors C29-C39 mount on the back of the board. Since C21-C28, on the front of the board, and C29-C39, on the back, are simply bypass capacitors connected between the supply lines and ground, they are omitted from the circuit diagram for clarity.**

# PARTS LIST

**Resistors** — all ¼W, 5%

| | |
|---|---|
| R1 - R4 | 10k |
| R5,6 | 4k7 |
| R7 | 22k |
| R8 | 330R |
| R9 | 100R |
| R10 | 330R |
| R11 | 150R (see note) |
| R12 | 120R |
| R13 | 220R |
| R14 | 470R |
| R15 | 4k7 |
| R16 | 10k |
| R17 | 2k7 |
| R18 | 150k |
| R19 | 47k |
| R20 | 150R |
| R21 - R25 | 10k |
| R26 | 330R |
| R27 | 1k |
| R28 | 4k7 |

**Capacitors**

| | |
|---|---|
| C1 | 10n |
| C2 | 470p |
| C3 | 220n |
| C4 | 1n0 |
| C5 | 22μ tantalum |
| C6 | 10n |
| C7 | 22μ tantalum |
| C8 | 82p |
| C9,10 | 1n0 |
| C11,12 | 2n2 |
| C13 | 22μ tantalum |
| C14 | 1μ |
| C15 | 20p |
| C16 | 68p |
| C18 | 10p (see note) |
| C17 | 100n |
| C19,20 | 22u tantalum |
| C21-C28 | 10n (see text) |
| C29-C39 | 10n (see text) |

**Potentiometers**

| | |
|---|---|
| RV1,2 | 50k trimpot |
| RV3 | 10k trimpot |
| RV4 | 50k trimpot |

**Semiconductors**

| | |
|---|---|
| IC1,2 | 7473 |
| IC3 | 74LS221 |
| IC4 | MCM6574 |
| IC5,6 | 74LS157 |
| IC7 | 74LS165 |
| IC8 | NE555 |
| IC9 | 7404 |
| IC10 - IC12 | 7493 |
| IC13 | 7490 |
| IC14 | 74LS153 |
| IC15 | 7493 |
| IC16 | 7400 |
| IC17 | 7486 |
| IC18 | 7474 |
| IC19 - IC21 | 74LS157 |
| IC22 - IC31 | 21L02-1 |
| IC32 | 74LS04 |
| IC33 | 74LS10 |
| IC34 | 8131 |
| IC35 - IC37 | 8097 |
| IC38,39 | CD4040 |
| IC40 | 74LS92 |
| IC41 | 74LS221 |
| IC42 | LM309K |
| Q1 | BC108 |
| Q2 | 2N2894 or 2N4258 |
| Q3 | BC108 |
| D1 - D11 | 1N914 |
| D12 - D15 | OA91 |
| ZD1 | 12 V, 400 mW zener |

**Miscellaneous**

| | |
|---|---|
| X1 | 12 MHz, HC18/U crystal |
| SW1 | 8-way BOSS or Utilux DIL switch |
| PCB | ETI 640 (see text) |

Heatsink for IC42, solder, wire, etc.

The first check is one that applies to all projects: a thorough inspection of the board and soldering, looking for bridged tracks or dry joints. Included in this inspection should be a check of the orientation of all components, especially IC's and tantalum capacitors, and the values of all discrete components.

Having ascertained that nothing looks amiss with the board the next step is to look at it at a more technical level. First check the voltage supplies to the board, the input to the voltage regulator (IC42) should have between +8V and +10V on it depending on your power supply and there should be about +16V on the bottom end of R26 (Zener dropper).

An easy place to check these two supplies after regulation and the −3V supply, which is generated on board, is on the pins of the character generator ROM (IC4). Pin 1 is (or should be) −3V, pin 2 is +5V, pin 3 is +12V.

Having checked the voltage supplies, the easy part is over and oscilloscope is almost mandatory from here on in. If you do not have a CRO think seriously about where you can acquire access to one.

With the aid of the CRO, the first thing to look for is output from the 12 MHz Master Oscillator (IC9). Pin 2 of IC9 should carry a 12 MHz square wave with an amplitude of at least 3.5V, which will probably look somewhat sinusoidal unless you have a wide bandwith CRO. If this output is missing check around the oscillator discrete components and the supply pins of IC9.

At this point we are assuming that no output at all is being obtained. If you already have a display of some sort you can skip various bits of this material as you think appropriate.

## Sync Pulse Generator

Next check for output from the Sync Pulse Generator. Pin 4 of IC41a should have a waveform like Fig 8 (negative going 5 μs pulse every 64 μs) and pin 12 should have a waveform like Fig 8a (negative going 300 μs pulse every 20 ms). If either of these waveforms is not present check the outputs and inputs of the dual monostable that is generating them. Note that actual voltage levels are extremely important in this area of the circuit as MOS chips are interfacing with LS TTL chips. In the prototype one MOS chip was encountered that would not sink its specified output current and hence the TTL chip being driven did not recognize a logic 0 (below 0.8 V).

A 2 MHz signal should be seen at pin 8 of IC40 (divide by six stage from the Master Osc.) then 15,625 kHz (period 64 μs) should be on pin 4 IC39. IC38 pin 12 should be 31,250 kHz and pin 14 should be 50 Hz (20 ms period).

If any output is not present check the input of the chip concerned, then if this is correct suspect the chip; but don't overlook the possibility of something else holding a short on its output. An easy way of checking for a short is to bend the output pin up (if sockets are used) and measure it completely open circuit.

Before speaking too harshly about any chip remember to check its supply voltage (and earth) and check that it is plugged in the right way round!

## Positioning Monostables

The vertical and horizontal positioning monostables (IC3a & IC3b) are triggered by the leading edge of Vertical and Horizontal sync respectively. The output of each of these monos should look like the input with the pulse width being dependent on the associated trimpot. The horizontal positioning mono is held reset when the End Of Page (EOP) flip flop is set, so if you are getting the correct output from the Horizontal positioning mono you can skip the next paragraph.

The Q output of the Vertical positioning mono is differentiated by R3, R4, & C1 to give a negative going pulse on the reset input of the EOP flip flop. (IC2a, pin 2). This pulse should look like Fig 8b. If this flip flop is not resetting check the discrete components in the differentiator. If the EOP flip flop is being reset correctly then the Horizontal positioning mono has no excuse for not working.

The End Of Line (EOL) flip flops (IC1b, IC2b) are reset by a differentiator similar to the one just described above (R1, R2, C2). The wave form on pin 6 of IC's 1b & 2b should be like fig. 4. The EOL ff's hold the entire counter chain when set, so it is necessary to obtain the correct output from both EOL ff's before venturing any further.

## Counter Chain

The first counter is the one which counts the bits across each character (IC13, 7490). This counter is wired to reset to zero when it reaches a count of nine and is inhibitted from counting (by the EOL ff) by having a reset nine (pin 6) held on it, which takes priority over reset zero. This counter is clocked at 12 MHz and the QD output (fig. 5) on pin 11 is used to load the shift register, clock the next counter (IC12) and clock the flipflops (IC18A and IC18B).

Remember that you will see gaps in the counter waveforms as they are inhibitted from counting for about 13 μs at the end of each line and also during the vertical blanking period for about 1 ms.

On the outputs of IC12 you should see a normal binary count, counting once for each character (each pulse from QD of IC13). This count should also be seen on the QB and QC outputs of IC11. The first (QA) and last (QD) flipflops in IC11 are not used.

As the QC output of IC11 goes low, (after the 64th pulse into IC12) it will set the first EOL ff (IC2B). (Check that the link, LK1, between IC11 and IC2B

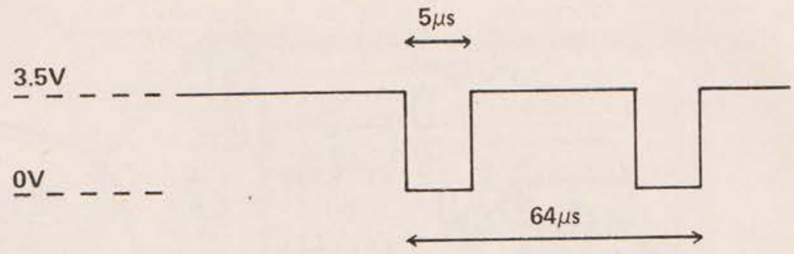



Fig 8. Waveform at pin 1 of IC41.

Note: logic '1' voltage could be between 3 volts and 5 volts

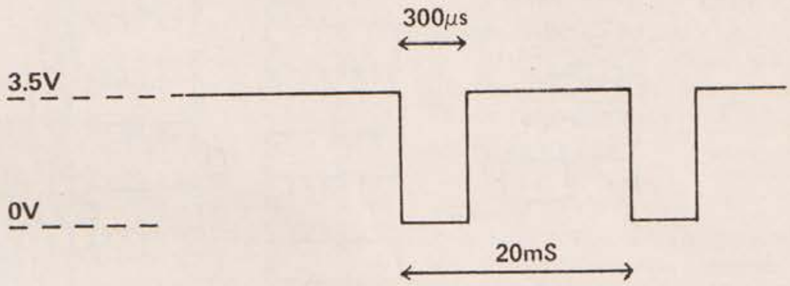



Fig 8a. Waveform at pin 12 of IC41.

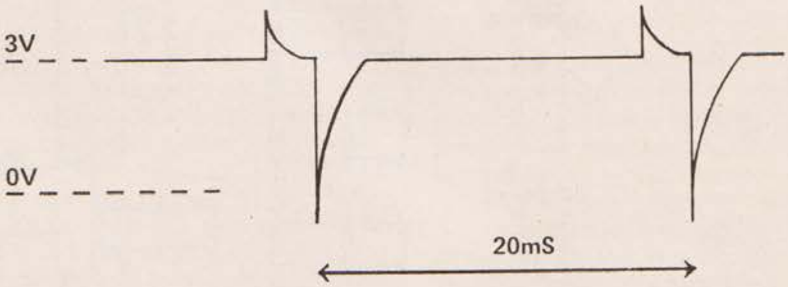



Fig 8b. This waveform should be seen on the reset input of IC2a (pin 2).

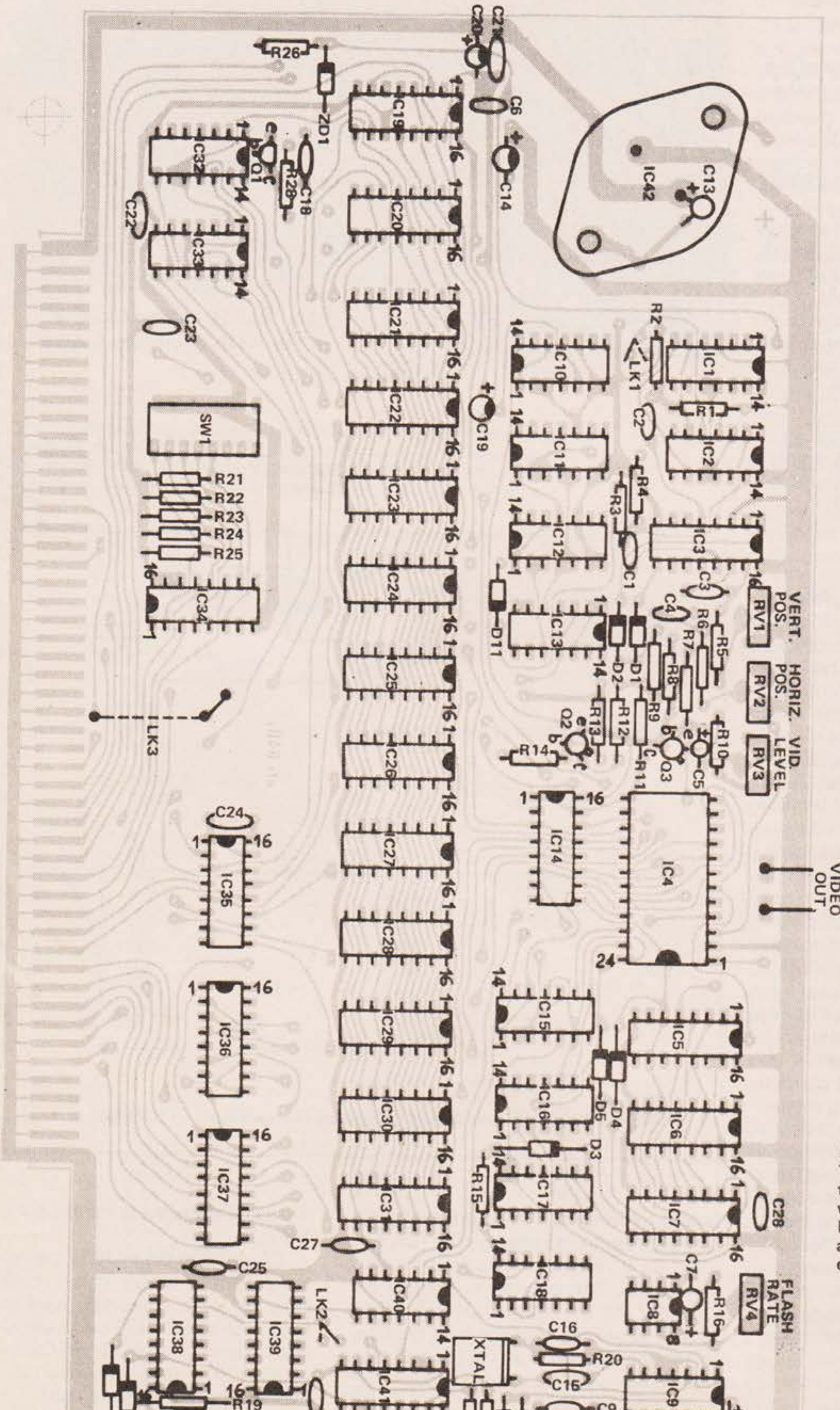



Fig 9. The component overlay. This shows the components on the top side of the board, plus C13 which is on the back of the board. It does not show C29-C39, which are mounted on the back of the board.

is installed). One character width later, the second EOL ff (IC1B) will set as the QC output of the first counter goes low.

The Row of Character counter (IC15, 7493) counts once every time IC2B sets, so on the Q outputs of IC15 you should see a binary count once every line (64 μs).

## Line of Screen Counter

IC10 is another 4 bit binary counter that counts which line of characters is being produced. It is clocked when IC15 reaches a count of 12 (via IC16/3).

Having ascertained that all the counters are working, the next thing to check is that the count is reaching the RAMs via the address multiplexers. The simplest way to do this is by a look at each address pin of the end RAM (IC31) (pins 1,2,4,5,6,7,8,14,15,16) ensuring that there is a waveform on each pin without worrying what the waveform looks like. Before doing this, however, check the select pin of any of the three multiplexers (IC19, 20, 21 – pin 1), which should all be logic zero. If they are not, the board is being addressed and a check around the board address decoding is required (see below).

## Bus Interface

Before looking at the video gating, SR and ROM, it may be desirable to check the interfacing to the bus so that known patterns of characters can be written into the RAM.

Firstly, write '00' Hex to the first location using your processor's monitor program and then read it back. Repeat this process with some other characters, or better still, write a simple program to write, then read, all 256 bit patterns to all locations in the first 1 K of the VDU. If the memory tests all right (i.e. what gets written also gets read) then you can skip the next section. Remember when checking the second K of memory that only the lowest order two bits are stored.

Select an address for the board, e.g. F000 – F7FF, (not F800 – FFFF) and put the processor in a loop reading from the first address of the VDU (e.g. F000). The output of the address decoder (IC34) should be normally high with a pulse going low every 20 μs or so in a typical system. The link connected to pin 7 of IC34 should be connected to earth.

Pin 12 of IC 33 should look almost identical to the previous waveform. If the program is now altered to read from the last location of the VDU, e.g. F7FF, the same waveform should be seen on IC33 pin 8. Change the program to write repeatedly to the first location and you should see a similar waveform on IC33 pin 6.

fig. 4.

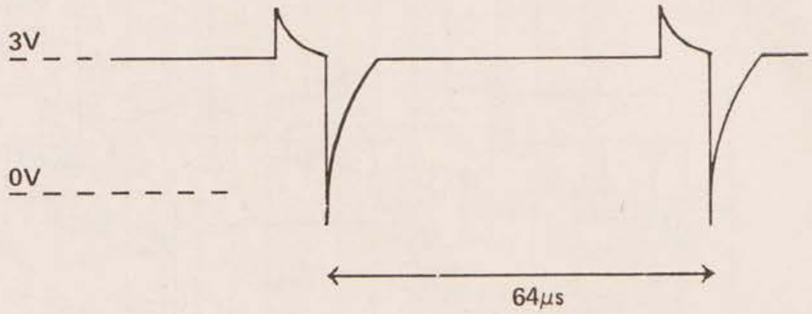



**Fig 10. The waveform on pin 6 of IC's 1b and 2b.**

Now fill the screen with an assortment of characters, by writing an incrementing count to each location; for example '00' in F000, '01' in F001, '02' in F002, etc.

Note: this can be done by altering the MOV M,A to a MOV M,L (75H) in the 8080/Z80 page clear routine.

If you put this pattern right through the second K of memory as well, every second character will flash and every second pair will be graphics.

The waveforms around the ROM and shift register are constantly changing, making it virtually impossible to trigger an oscilloscope, but this doesn't matter as the actual waveforms are not important. As long as a changing waveform with suitable amplitude (3.5 – 4 V) is seen on all appropriate pins then all is well.

All the address pins to the ROM should fall into this category. Check pins 4, 8, 9, 11, 12, 15, 16 of IC4. If any pin is found to be held either high or low or if the amplitude is less than 3 V then look for shorts around this pin.

Continue checking all inputs and outputs of the multiplexers (IC's 14, 5, 6) and the inputs of the SR (IC7). On the output of the SR (pin 9) you should see a waveform that begins to resemble a video signal, i.e. a constantly changing waveform with gaps at horizontal and vertical blanking rates.

## Inverse Video

The digital information is inverted by IC17 to create black on white characters. If any problems exist in this area check around the D flipflop (IC18A).

The output from the BOW inverter (IC17 pin 8) has the blanking added to it by the diode OR gate (negative logic) from the second EOL ff IC1B. The output is also forced to black at this point by the transistor whenever the processor accesses the VDU. If this point (IC16 pin 12) is being held low, lift the diode to IC1B and the collector of the transistor in turn to isolate the cause.

## Flashing

The signal is forced to black whenever a flashing character is being accessed but not displayed by IC16/2. If there is no output or a character cannot be selected as flashing, check that the 555 (IC8) is producing a 2 Hz square wave on pin 3 and that all signals around the D flipflop appear normal.

## Video and Sync Combiner

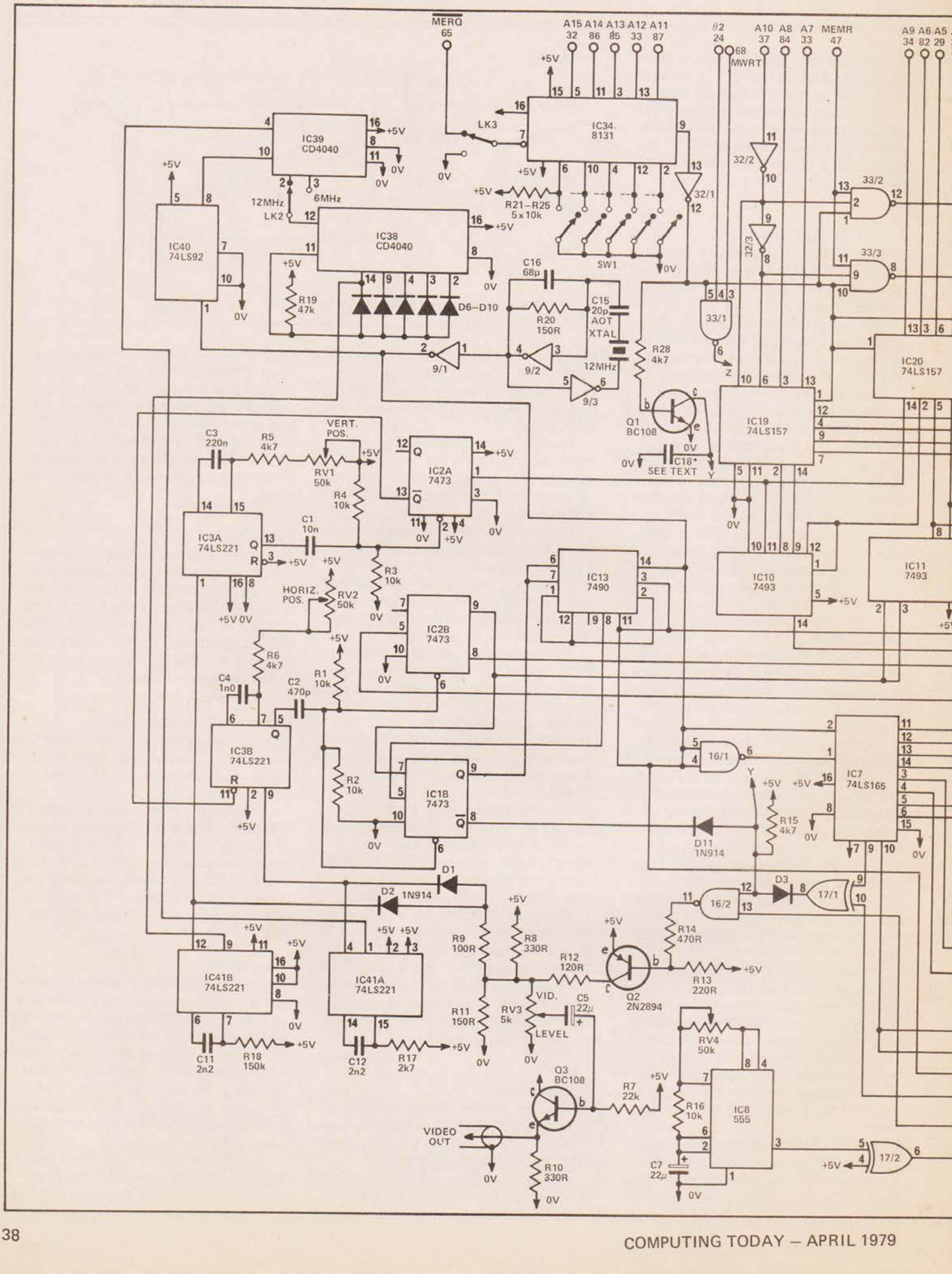
The only thing that stands between this point and a genuine composite video signal is a handful of discrete components.

A composite video signal is nominally 1 V peak to peak (i.e. from the bottom of sync to the top of white level) and syncs comprise only about 0.3 V of this overall 1 V. It is possible to wind the output level up to about 4 V using the 'video level' trimpot if your monitor needs this much drive.

## Conclusion

The approach outlined above is really just a logical approach to faultfinding any digital circuit; start at one end and work to the other until a chip is found that is not producing the correct output for the given input. Normally it is not necessary to go through the entire circuit in this fashion as an educated guess can put the fault in a particular part of the circuit.

Remember, every minute of care taken in assembly is worth hours of debugging. Good luck and good hunting.


MERQ
IC39 CD4040
IC38 CD4040
IC40 74LS92
IC34 8131
LK3
LK2
12MHz
6MHz
R21–R25 5 x 10k
SW1
D6–D10
R19 47k
C16 68p
R20 150R
C15 20p AOT
XTAL 12MHz
R28 4k7
Q1 BC108
C18* SEE TEXT
IC19 74LS157
IC20 74LS157
IC10 7493
IC11 7493
IC13 7490
IC2A 7473
IC2B 7473
IC1B 7473
IC3A 74LS221
IC3B 74LS221
C3 220n
R5 4k7
VERT. POS.
RV1 50k
R4 10k
C1 10n
R3 10k
HORIZ. POS.
RV2 50k
R6 4k7
C4 1n0
C2 470p
R1 10k
R2 10k
IC7 74LS165
R15 4k7
D11 1N914
D1
D2 1N914
D3
IC41B 74LS221
IC41A 74LS221
C11 2n2
R18 150k
C12 2n2
R17 2k7
R9 100R
R8 330R
R11 150R
RV3 5k
VID. LEVEL
C5 22μ
R12 120R
Q2 2N2894
R14 470R
R13 220R
Q3 BC108
R7 22k
VIDEO OUT
R10 330R
RV4 50k
R16 10k
IC8 555
C7 22μ
+5V
0V

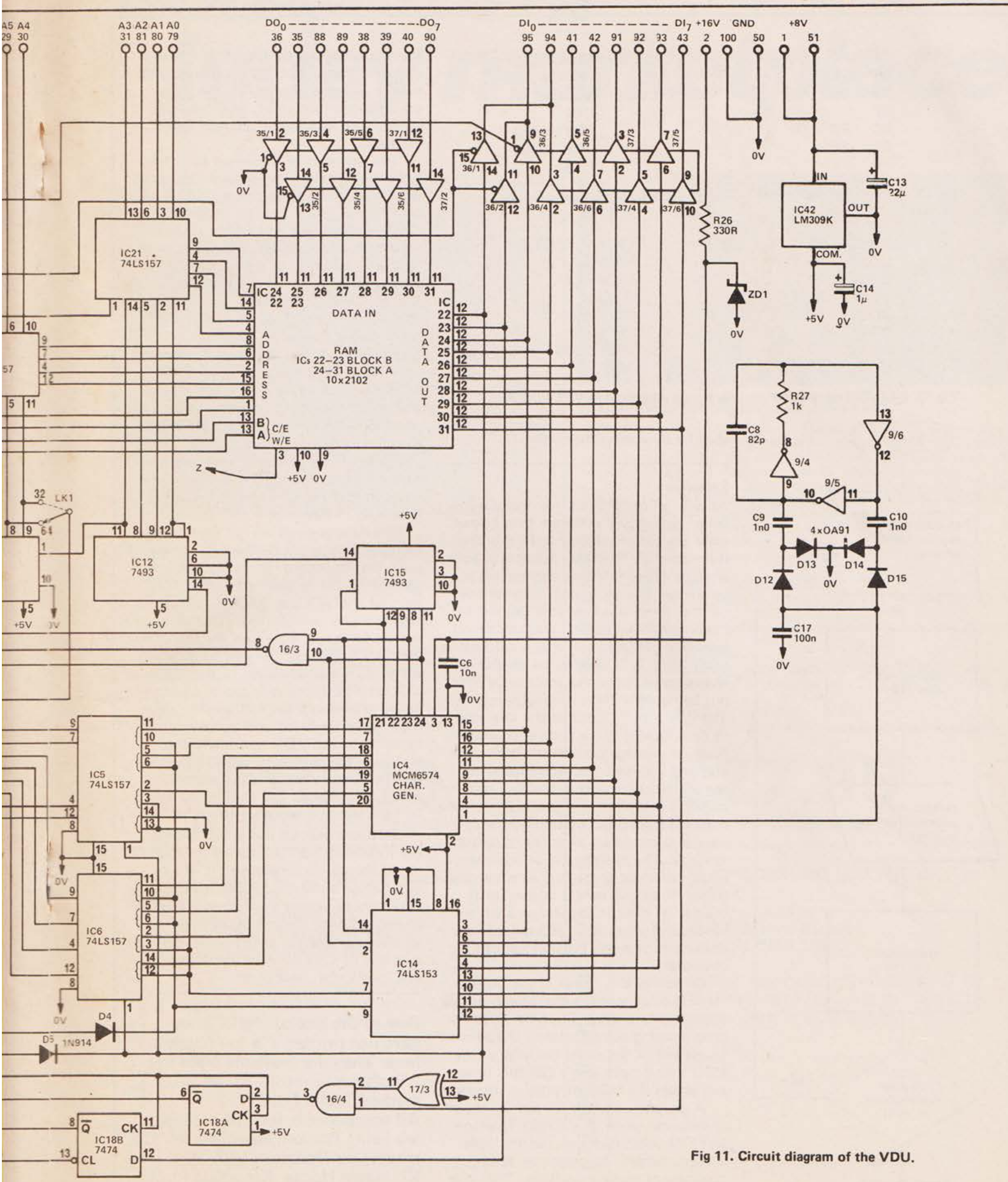



Fig 11. Circuit diagram of the VDU.

```
CE  F0  00              LDX F000
86  20                  LDA A   20
A7  00           LOOP:  STA A   X
31                      INX
8C  F8  00              CPX F800
26  F8                  BNE LOOP
39                      RTS
```

**Fig 12. 6800 screen clear routine. This is not located at any particular address.**

```
B000  21  00  F0     LXI  H  'F000'
B003  3E  20         MVI  A  '20'
B005  77             MOV M,A
B006  23             INX  H
B007  7C             MOV A,H
B008  FE  F8         CPI  'F8'
B00A  C2  03  B0     JNZ  B003
B00D  C9             RET
```

**Fig 13. 8080/Z80 screen clear routine, shown assembled to start at B000.**

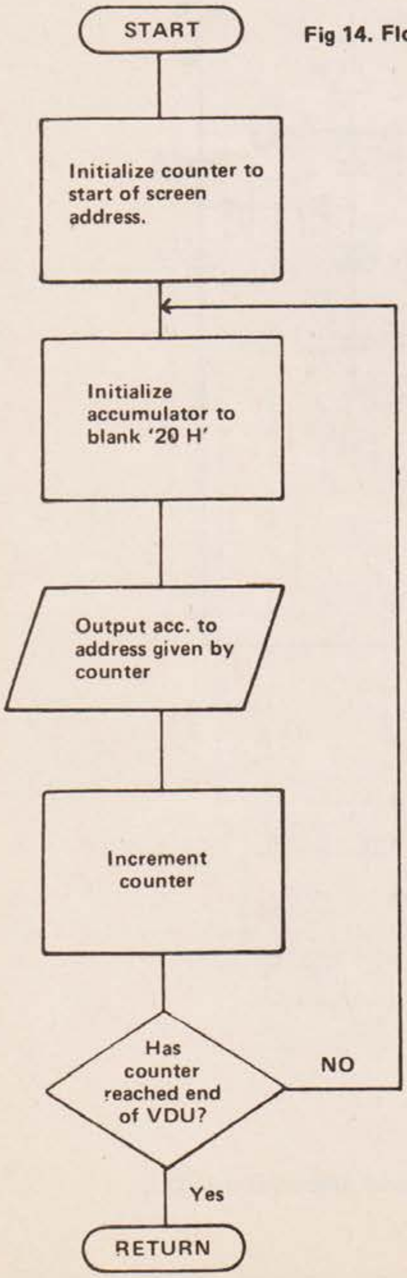



**Fig 14. Flow chart for the screen clear routine.**

## Software

As with all peripherals it is necessary to have some driver software that knows what the peripheral wants. In this case it is necessary to keep a counter in software of where the next character is to be written and to do decoding for any control functions that it is desired to implement. The normal way this driver would be used is to call it as a subroutine every time it is desired to output a character with the character to be output being passed in a particular register. The driver then looks at the character to determine if it is a control character (such as carriage control, or backspace etc) and if it isn't then it is placed on the screen at the cursor position and the cursor is moved on one place. Since the cursor is something written by the software you can select a variety of cursor symbols. The most useful being to use a black on white character, so when the cursor is sitting over a blank (as it usually is) then it appears as a white block, and when it is backspaced over characters, it is still possible to read the character.

Of course this driver is the normal method of outputting characters, simply operating as a 'glass Teletype' with no programming complications. If you wish to use any of the other facilities of the VDU you simply don't call this driver and access the VDU directly as memory.

A program written for some special application, such as a Radio Teletype (RTTY) substitute can use multiple cursors simply by keeping several counters of output position. Thus one area of the screen could be reserved for incoming messages while another area is outgoing message preparation area with maybe a line at the top of the page giving log information, like callsign, name, and location of station being worked.

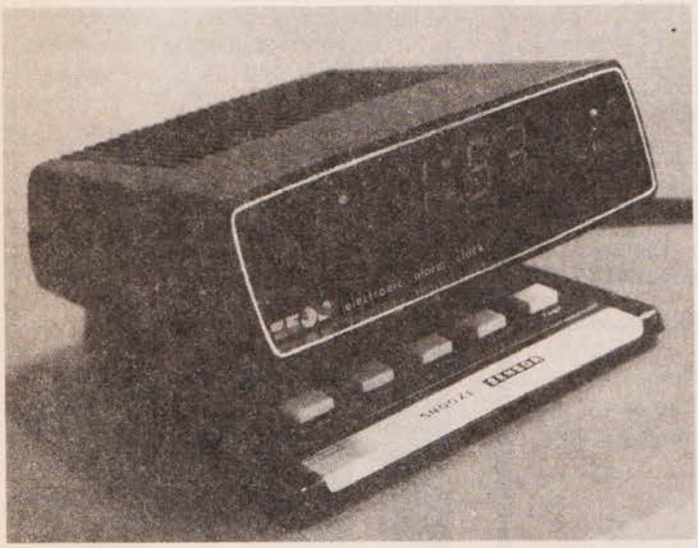
The first part of the driver software, which it becomes immediately obvious is necessary, is a screen clear routine, as the VDU displays chaotic conglomeration of characters and graphics when it is first powered up. This routine is very simple as all it needs to do is write blanks all over the screen and set the flashing and graphic bits for each character to zero. The ASCII code for a blank is 20H and the flashing and graphic bits are the two least significant bits, so if the program writes '20H' 1024 times to make the screen blank and then continues to write '20H' another 1024 times to eliminate any graphics or flashing characters then our object has been achieved. The program to do this can be written in a lot less space than it takes to describe it, see the flowchart in figure 14.

The listings given are not minimized completely but are written to agree with the flowchart for clarity. As you can see all the programs refer to the start of the VDU as 'F000H', this is where I have located the VDU in my system so that it is up near the top of memory and out of the way of program space. It is not advisable to put the VDU at 'F800', the very top of memory, as the processor's bus will usually 'float high' when tri-stated and hence attempt to write to the VDU and blank the screen. If the choice of 'F000H' doesn't conflict with your existing memory map I recommend you use this address to facilitate any software interchange.

Software beyond this is best left to the individual constructor, as everyone has different requirements. It is not difficult to write the simple routines necessary to update the cursor and write characters onto the screen, but there are so many processors in use at present that it is of little value to give them for one particular processor.

**Due to the size of the PCB we have not printed the foil patterns here. They are available from the CT offices in return for an SAE marked 'VDU Foils'.**
**All components for this project are being stocked especially for CT readers by Marshalls Ltd. of Kingsgate House, Kingsgate Place, London NW6 4T4.**

# computing today marketplace



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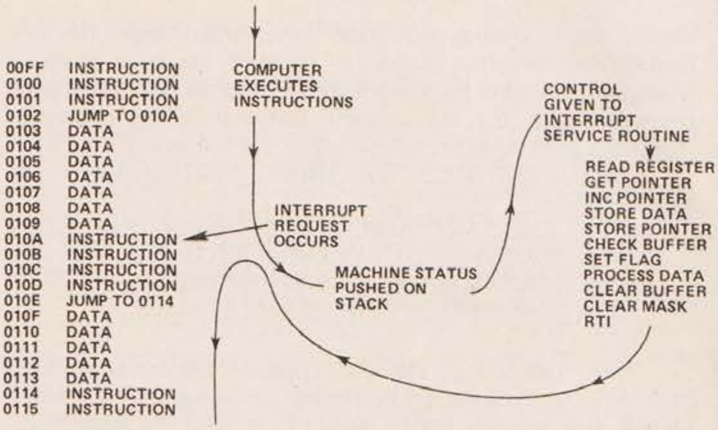



Last month we finished up by discussing how a computer can send data to a peripheral device by occasionally checking a READY bit in the device's STATUS REGISTER to see when the device is ready to send or receive more data. This PROGRAMMED type of I/O transfer is a very simple method of communicating with peripherals and is all that is needed for most hobbyist uses involving simple operations based around a teletype machine and a paper tape or cassette storage system.

However, as a system becomes larger, with many more devices such as extra teletypes, magnetic tapes, or maybe even small discs, the many disadvantages of the programmed transfer far outweigh its only advantage (it simplifies programming) and the many different things that have to be taken into account with all sorts of devices operating at different speeds even tend to make this type of programming more complicated. In a large system, so much thought would have to be put into program design to ensure that data is not lost because the computer didn't check for them in time, that it is not practically feasible to design such a system.

### The interrupt

If the computer had nothing else to do anyway, it might just as well sit around waiting for the peripherals, but if the peripherals supply it with enough information, then the chances are that it will need all of its computing power doing operations on that information before the peripheral supplies more. In such a case, it would be very efficient if it didn't have to concern itself with the peripheral at all until the peripheral is ready to send or receive more data. In this way, time normally spent looking a the peripheral's status register could be put to better use on a calculation. Such a method exists in all computers and microcomputers (most modern systems could not do without it) and is called the INTERRUPT–DRIVEN transfer. What generally happens is this:

a) Before the computer expects any data from a peripheral, it sends a code to the device giving it the ability to interrupt.

b) At a later point in time, the computer will decide that it needs some data from a peripheral. Let's say it decides it wants the cassette recorder to start its motor and read in data. The computer will send a code to the cassette recorder telling it to do this. Once this is done, the computer makes a note that this operation has been initiated, and does something else. It does NOT have to keep checking the status bit in the cassette interface to see if the latter is ready. If the computer runs out of operations to be completed, and has nothing more to do, then it merely executes a WAIT FOR INTERRUPT instruction.

c) The logic in the cassette interface will do the operations necessary to start the cassette and begin reading the data stored on it. When it has a byte of information ready, it signals the processor via an INTERRUPT line. When the interrupt line is active, the processor completes any instruction that is in process, stops operation of the main program, and goes to a separate program in memory that is designed to read a byte of information from the cassette interface.

d) When the INTERRUPT SERVICE routine has completed its work (ie, one byte has been taken from the cassette interface and stored in an appropriate place in memory) it will execute a RETURN FROM INTERRUPT (RTI) instruction.

e) When the processor sees the RTI, it will immediately resume operation of the main program from where it left off.

### The stack

One fine point that was omitted from the above description of how an interrupt occurs is called "SAVING THE ENVIROMENT". While the main program is running, temporary values are stored in the various registers built into the processor. If the interrupt service routine has to use the same registers, then what will happen to the data that were in them when the main program was interrupted? The answer to that question is obviously that they would be lost, or written over, were it not for the operation of the STACK and STACK POINTER.

The stack is a predetermined area in memory where temporary variables can be stored away when they are not in current use. The stack pointer is one of the processor's internal registers which helps keep track of which stack location is the next one to be used. At the very start of the operation, the STACK POINTER is INITIALISED (ie, preset) to the address which is at the TOP (or highest–numbered location) of the space designated as the stack in memory. Every time a command is received by the computer to put something onto the stack, it puts it in the location whose address is stored in the stack pointer, and then automatically decrements the stack pointer, causing it to point to the next lower location on the stack, which is not the highest free location.The above operation is called PUSHING on the stack. The reverse happens when data are read off the stack (POPPING). In the latter case, the stack pointer is first incremented by one, and then the data is read out of the location pointed at by the new value of the stack pointer; In the case of most modern computer designs, some or all of the enviroment is automatically pushed onto the stack when an interrupt occurs. An important point to remember is that if six items are consecutively pushed onto the stack, and then popped off, the last item to be pushed will be the first one popped, because it will still be pointed at by the stack pointer. For this reason, the stack is called a FIRST–IN, LAST–OUT buffer.

Let's go back to our original example, where the computer is merrily running its main program (sometimes called the MAINSTREAM of MAINLINE coding), using the M6800 as our example, (although other micros do it in a similar way). During execution of an instruction, the interrupt line becomes active (ie, its state has been changed from the idle state by some external means). At the end of the operations for the current instruction, the processor stores the environment, consisting of the following:

1000 ADDRESS OF NEXT INSTRUCTION IN MAINLINE
FFE CURRENT VALUE OF INDEX REGISTER
FFC CONTENTS OF ACCUMULATOR A
FFB CONTENTS OF ACCUMULATOR B
FFA CONDITION CODE REGISTER

The numbers at the left represent the actual address in which the data would be stored, assuming that the stack pointer was initially set to 1000. Note that the ADDRESS and INDEX REGISTER both occupy two bytes each. This is because they are 16–bit values and the memory is only 8 bits wide.

Now that all values are stored away, control can safely be given to the interrupt service routine without worrying about losing valuable data. The interrupt service routine now has complete and unhindered use of the machine. However, there are two golden rules which it must obey:

1) It must not tamper with the data stored in the current stack, ie, those locations higher than the current stack pointer but lower than the top of the stack.

2) It MAY push additional values on the stack if it needs to, but it must POP them off before it gives control back to the MAINLINE. The reason for this is that when the RTI instruction is processed it will assume that the stack pointer is exactly the same as when the interrupt routine was entered, and will reload all the machine registers with the values stored in positions relative to the current stack pointer, and if the stack pointer is changed then all these values will be wrong.

For the above reason, all interrupts must end with an RTI instruction, to ensure that all registers are properly reloaded with their original values before control is given back to the MAINLINE.

At the point where the mainline gets control again, the machine will be in exactly the same condition as when control was taken from it, and it can carry on operations just as if nothing had ever happened.

## Masked and non–maskable interrupts

In some cases, the programmer may not want some devices to interrupt the program. For instance, suppose a system has a real–time clock, interrupting the system every 1/10 second, and a teletype machine, interrupting also every 1/10 second. For reasons of timing, the programmer may always want to receive the clock interrupt at exactly the same time as it happens, but may want to delay acknowledgement of the teletype interrupt until it is ready to handle it. The clock is then connected to a pin on the processor chip called NON–MASKABLE INTERRUPT, (NMI). The teletype is connected to a pin called MASKABLE INTERRUPT REQUEST (IRQ).

The NMI always causes an interrupt process, and is always acknowledged, but the microprocessor has internal circuitry to prevent the IRQ from having any effect, if the internal INTERRUPT MASK bit is set in the condition codes register. This bit can be set and cleared using the SET INTERRUPT MASK, and CLEAR INTERRUPT MASK instructions. Thus if the INTERRUPT MASK is set, and the teletype causes an IRQ, no action is taken by the program. However the IRQ will remain active until it is dropped by the TTY controller, and so if the computer executes a CLEAR INTERRUPT MASK instruction, it will immediately go into an interrupt sequence.

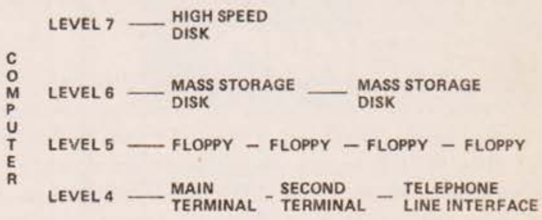



Fig 2. Levels of priority within a system.

## Setting priority

The above operation is the simplest form of a priority system. There are two so–called PRIORITY levels in the system, NMI (the higher) and IRQ (the lower).

In more sophisticated computers, a need arises for more than two priority levels in an interrupt system. For instance, on a minicomputer system, there may be high–speed swapping disks, a medium–speed mass–storage disk, a few floppy disks and several teletype terminals. The very high speed disk must be acknowledged immediately, or data might be lost as new data arrives very fast due to the rotational speed of the disk. Thus this device will be attached to the highest priority line. The other disks will be assigned to other priority lines in order of their speed, with teletype terminals taking the lowest priority because they are the slowest. (See Fig. 2.)

You will notice from Fig. 2 that similar devices are connected to the same priority line. This does not exactly mean that they enjoy the same priority, since the devices which are closer to the computer can prevent devices further away from interrupting. Therefore they can create a second kind of priority, not controlled by the computer and called LATERAL PRIORITY, or HORIZONTAL PRIORITY. (The priority gained from the priority levels 7 through 4 is called VERTICAL or MACHINE PRIORITY.) Notice that the main terminal is closer to the computer than the communications line.

Together with the various levels of priority is an internal register called the PRIORITY REGISTER. This register contains a number, which is, in effect, like an INTERRUPT MASK, as described earlier. If this register is set to 6, then only devices of level 6 priority and higher will be acknowledged when they try to interrupt. To allow the teletype to interrupt, the computer will have to change the machine priority level to 4 or lower. This is very useful when transferring large amounts of data between fast devices and memory, to prevent slower devices gaining control of the machine at critical times.

## Polling vs vectors

The interrupt service routine is entered by what is known as a VECTOR ADDRESS. A VECTOR ADDRESS is a pre–defined address that is jammed into the program counter after the environment has been saved during an interrupt. It is generated by the computer in most small systems, but in more sophisticated systems it can be specified EXTERNALLY, by the peripheral.

In our example the M6800, there are only two vector addresses that can be used for hardware interrupts. One is for the NMI and the other is for the IRQ. These values are stored in some of the upper memory locations. This means that if five devices can cause an IRQ, then every time an IRQ occurs, the interrupt service routine must POLL, or ask each device if it was the one that caused the interrupt. The disadvantage of this system is that it takes alot of time, but for the small system user this is of little consequence, because an externally–specified vector system, while many times faster, is much more expensive in terms of the extra logic needed in the peripheral controllers.

In the externally–specified vector system, each device that can interrupt is given its own program in memory to handle its requests for service. (This is not a waste of space, since each device would need its only special code anyway.)

When an interrupt is recognised by the computer, an INTERRUPT GRANT signal is sent out for the priority level that has caused the interrupt. If a device receiving the GRANT signal was the one that started the interrupt process, then it will respond to this grant signal by sending the computer its vector address. If not, it merely passes the GRANT onto the next device along the bus at the same priority level. In this way, devices of the same MACHINE priority level have greater LATERAL priority if they are connected closer to the computer, as was shown earlier.

## Transfers without the computer

Some computers have the ability to be stopped dead in their tracks by an external device. This external device such as an ultra–high–speed disk or large off line memory, can pull down the HALT line to the computer. The computer will then halt immediately, ie, without waiting for the end of an instruction, and the external device will have complete control of the bus. When it gets control, then it can do mass transfers of large blocks of data simply by supplying all the address and control signals that the processor normally supplies.

Such data transfers can happen at the maximum speed of the memory, since they are unhindered by the fact that the program has to load and store each location. This method is called DIRECT MEMORY ACCESS, and is the most efficient way to transfer large amounts of data. However it has a drawback–it is very expensive in terms of hardware when compared to the simple program controlled method, since large amounts of hard logic are required in each peripheral that has this capability. This logic is needed to keep track of addresses and timing signals, since the processor cannot supply these. For this reason, DMA is used only where large amounts of data are being transferred all the time between high speed devices. In the next article in this series, we will look into some of these types of devices.

# HOME COMPUTER SURVEY

By Ian Graham

As small computer systems go the way of all mass—produced microcircuitry of late i.e down in price, manufacturers are beginning to find the hobbyist/small business applications a lucrative market.

This month we look at eight readily available mini—computer systems of interest to the hobbyist, ranging in price from £165 for the Nascom 1 kit to £1205 for Apple II with a TV monitor (£985 without monitor). Prices for higher level versions are also included.

For ease of comparison, we have listed the information in the same format for all systems. Basic information on applications, the hardware you get for your money, memory capacity, video display and extra hardware available is given. Where the basic system does not include a TV monitor, we have added it on to the price. In other words, when you shell out the price listed, you have a complete system, ready to go.

In most cases extra hardware is available. Where the range of add—on units is extensive, we have given just a few examples to illustrate the range.

Data transfer figures are given in baud. Although the baud is now synonomous with bit per second, it wasn't always that simple. The baud used to be defined as the number of Morse code dots transmitted continuously in a second. (No, it doesn't mean a great deal to me either). The higher the data transfer figure, the quicker the system will load a program from cassette, or floppy disc if specified.

These minicomputers are by no means intended solely for the home computing market. Indeed, one or two which were designed specifically for hobbyists have found their way into small business applications. In some cases scientific, business, financial and/or educational programs are available on prerecorded cassettes.

Hardly a week goes by without one manufacturer or another announcing a new add—on or an improved basic system or a change in retail price of an existing system. As we hear of these changes we'll keep you posted in our news pages.

When you have decided which system is ideal for you, how do you get the most from it? Users' clubs, springing up all over the country, provide a forum for computer owners of all abilities, from novice to experienced programmers, to exchange ideas and programs. Details of Users' clubs, their meetings and facilities available are published from time to time in Computing Today.


**SYSTEM:** Micros
**SUPPLIER:** Micronics,
1, Station Road,
Twickenham,
Middlesex
Tel: 01–892–7044.

**PRICE:** Kit + VDU £455
Assembled + VDU £494.

**APPLICATIONS:** Small business, process control, hobby. Yet another system based on the Z80 CPU. The basic hardware includes keyboard, power supply and TV, video monitor, cassette and printer interfaces. Micronics can also supply a display unit. Two TTL compatible I/O ports are provided. Two further parallel I/O ports are optional.

**MEMORY:** 2K RAM
1K EPROM monitor
2K BASIC EPROM with either 4K RAM or 8K RAM are available on extra boards. The Micronics expansion unit provides extensions up to 64K memory. There is an extra 1K EPROM socket on the main board, and 4K EPROM sockets on an optional board. Up to 10K RAM and 6K EPROM can be accommodated internally.

Micros may be programmed at machine level in Z80 code or at high level with the BASIC interpreter, supplied on cassette or as a set of plug–in EPROM.

**VIDEO:** 768 character display, 16 lines by 48 characters. 128 ASCII characters on a 9 by 7 matrix.

**HARDWARE AVAILABLE:** 5¼ inch mini–floppy drive and controler. Display unit. Acoustic telephone coupler, 40 column impact printer.

**DATA TRANSFER RATE:** Standard 250 baud. An upgraded version giving 2400 baud will be available in the near future.

**SYSTEM:** PET 2001–8
**SUPPLIER:** Commodore Systems Division,
360, Euston Road,
London.
Tel: 01–388 5702

**PRICE:** 2001–4 (4K RAM) £496.80
2001–8 (8K RAM) £594
2001–16N (16K RAM) £729
2001–32N (32K RAM) £858.60
Prices include VAT.

**APPLICATIONS:** Hobby, commercial, science, education. PET may also be used as a front and end processor, in several languages for linking to a mainframe computer. PET is a single unit based on the 6502 CPU and IEEE–488 interface, comprising screen, cassette recorder and keyboard (73 keys plus 20 key calculator pad). The 16N and 32N models will be available from May '79.

**MEMORY:** 8K RAM, expandable to 32K externally.
8K ROM BASIC interpreter (extended BASIC)
4K ROM operating system
1K ROM diagnostic routine
1K ROM machine language editor.

**VIDEO:** 9 inch CRT, 1,000 character display, 40 column by 25 lines, 8 by 8 dot matrix (characters and continuous graphics. Reverse field on all characters.

**PROGRAM LIBRARY:** Scientific, financial, business, educational and games cassettes are available from Commodore and other software companies.

**DATA TRANSFER RATE:** 1,000 baud, but with built–in software any program is recorded twice in series for reliability, cutting the effective rate down to 500 baud.

**HARDWARE AVAILABLE:** In April '79 Commodore are introducing two new printers. The 2023 is an 80 column seven by six needle matrix impact printer with an average printing rate of 93 characters per second. The 2022 is a high quality tractor feed printer, the professional version of the discontinued 2020. The PET second cassette deck plugs directly into the PET 2001 computer and the functions are under program control. The 2040 dual drive floppy, available in May '79 will complete the system.

**SYSTEM:** APPLE II
**SUPPLIER:** Personal Computers Ltd.,
18–19, Fish Street,
London. EC3.
Tel: 01–283–3391.

**PRICE:** 16K + TV monitor £1205

**APPLICATIONS:** Education, hobby, science, finance. Apple II is based on the 6502 MPU. It includes an ASCII keyboard, cassette interface, peripheral connectors, loud–speaker, game I/O connector and two game controls. Audible cues announce system functions or programming errors, and make games more interesting.

**MEMORY:** 16K RAM (up to 48K available)
6K ROM BASIC
2K ROM monitor.

**VIDEO:** Personal Computers can supply a 13 inch colour television monitor. The 5 by 7 matrix upper case characters are displayed on a 40 character by 24 line picture. Normal, inverse and flashing characters are provided. Graphics are available in 15 colours.

**DATA TRANSFER RATE:** 1500 baud.

**HARDWARE AVAILABLE:** 16K RAMS and ROM boards, graphics joystick, voice recognition card, cassette recorder, 5¼ inch floppy disc subsystem, Centronics printer – just a few from PC's extensive range.

**SYSTEM:** TRS–80
**SUPPLIER:** Tandy Corporation,
Bilston Road,
Wednesbury,
West Midlands.
Tel: 021–556–6101.

**PRICE:** Level 1 (4K) £499
Level 1 (16K) £728
Level 11 (4K) £578
Level 11 (16K) £807

**APPLICATIONS:** Level 1 Hobby and education
Level 11 Small business

The system based on the Z80 CPU, comprises four units–mains/battery cassette recorder, VDU, power supply and the CPU.

**MEMORY:** 4K RAM program storage (level 11 12K)
1K RAM (static) for video display
4K ROM

**VIDEO:** 12 inch CRT. 1024 character locations, 64 columns by 16 lines. Each character location can be sub–divided into a 2 by 3 matrix, giving an overall 128 by 48 matrix. The 6144 positions can be individually lit or dimmed from program to produce continuous or interrupted graphics.

**DATA TRANSFER RATE:** Level 1 250 baud
Level 11 500 baud.

**SYSTEM:** Exidy Sourcerer
**SUPPLIER:** Teleplay,
14 Station Road,
New Barnet
Herts. EN5 1QW.
Tel: 01–441 2922

**PRICE:** 16K £760 + VAT
32K £950 + VAT

**APPLICATIONS:** Hobby process control, invoicing. Based on the Z80 CPU, this system is a single unit containing CPU, RAM, monitor, keyboard and modems. (modulator/demodulators) for TV and tape recorder. The keyboard is 63 key qwerty with a 16 key numeric pad. Dual cassette I/O and parallel port for direct Centronics printer attachement are supplied.

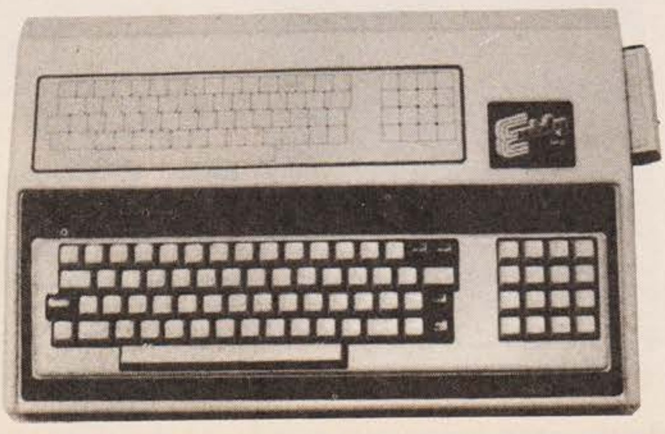
**MEMORY:** 16K RAM (32K available)
12K ROM

A socket on the side of the case allows the insertion of 8K of ROM in cartridge form. The plug–in ROM cartridges contain programming languages such as Standard BASIC, Assembler and Editor, operating systems such as DOS (Disc Operating System), enabling Fortran and Cobol to be used, and applications packages such as Word Processor.

**VIDEO:** The video output, which can be turned into UHF for a few pounds, produces a 64 character by 30 line picture (8 by 8 dot matrix).

**DATA TRANSFER RATE:** Remote computer control at 300 and 1200 Baud.

**HARDWARE AVAILABLE:** An S–100 expansion unit is available allowing further machine expansion.



**SYSTEM:** NASCOM 1
**SUPPLIER:** Nascom Microcomputers,
92, Broad Street,
Chesham,
Bucks.
Tel: 02405 75151

**PRICE:** Kit from £165.00.

**APPLICATIONS:** Games, maths. You'll need a soldering iron, a power supply and a domestic TV to turn this Z80 microcomputer into a working system, with an ordinary cassette recorder for program storage. A suitable power supply should give +12 V at 150 mA
+5 V at 2 A
–5 V at 90 mA
and –12 V at 12 mA (for RS232 only)

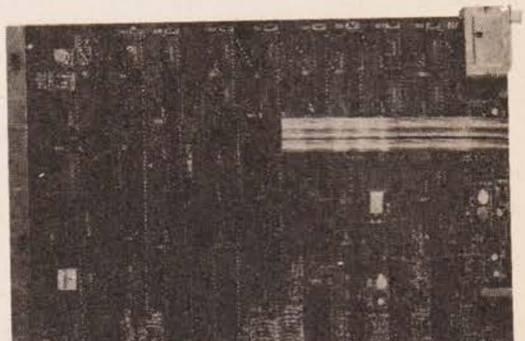
The kit includes a Z80 CPU, an uncommited PIO, a TV modulator, an assembled keyboard, an IM 6402 UART, memory, cassette or RS232 interface, a double–sided PCB, all other passive and active components, wire, solder and complete documentation.

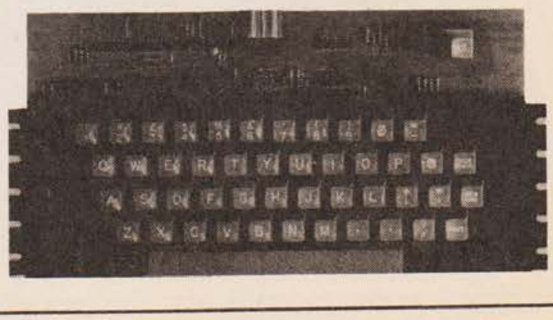
**MEMORY:** 2K RAM static
1K monitor (in a 2708 EPROM)

**VIDEO:** The format is 48 characters by 16 lines. The video should be blanked during VDU RAM access by the CPU, However the blanking signal is not long enough, so noise creeps through, appearing as snow on the screen. This problem can be corrected by using the circuit shown in the Nascom 1 review in the November issue of Computing Today (ETI supplement).

**DATA TRANSFER RATE:** Tape 300 baud, floppy disc 256k baud.

**HARDWARE AVAILABLE:** Suitable power supply,4K and 6K memory boards, BASIC interpreter, I/O board, NASBUS motherboard.





**SYSTEM:** HORIZON
**SUPPLIER:** Comart,
P.O BOX 2,
St. Neots,
Cambs.
Tel: 0480 215005.

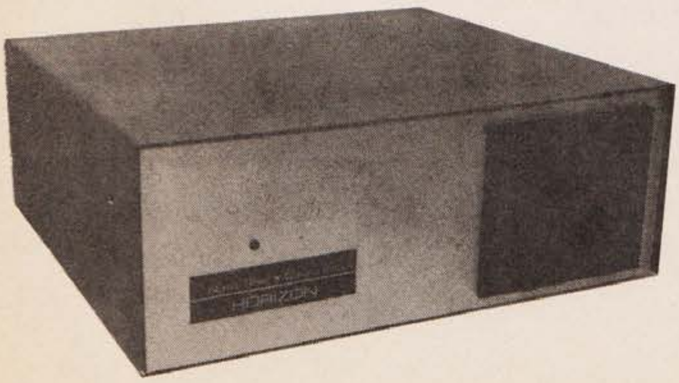
**PRICE:** From £995

**APPLICATIONS:** Education and small business. This Z80 system comes with integral floppy dic drive and controller, and an interface for any V24 or current loop interface terminal. The Horizon motherboard has slots for up to 12 S–100 circuit boards, which can be powered by Horizon itslef. The seriel I/O port and disc drive power regulation circuitry are included on the motherboard.

**MEMORY:** 16K RAM
One mini disc drive with 90K
(Maximum 48K memory with three discs). Horizon includes North Star extended disc BASIC and DOS on discette. The disc controller board can control up to three drives. The Horizon software discette also includes a comprehensive monitor and memory test for hardware and software maintenance.

**DATA TRANSFER RATE:** 125K Baud.

**HARDWARE AVAILABLE:** Extra serial and parallel I/O interfaces may be added for a printer, second terminal, or modem requirements.




**SYSTEM:** 380Z
**SUPPLIER:** Research Machines Ltd.,
P.O. BOX 75,
209, Cowley Road,
Oxford.
Tel: 0865 49792.

**PRICE:** 16K system £965 + VAT.

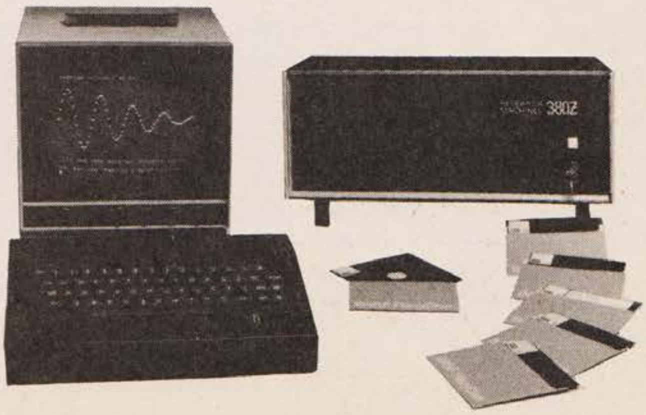
**APPLICATIONS:** On–line data logging and control, educational, scientific research. The system is based on the Z80, and used CP/M software. The smallest system available has 4K memory, 380Z processor and keyboard.

**MEMORY:** 4K (Maximum memory capacity currently available is 56K). The software available includes BASIC interfaces, Z80 Assembler, interactive text editor, terminal mode software, data logging routines, CP/M DOS (Disc Operating System), text output processor, CBASIC compiler, Fortran, Algol, Pilot, Cobol, CP/M users club library.

**VIDEO:** The integral VDU interface gives upper and lower case characters and loe resolution graffics. Text and graffics can be mixed anywhere on the screen. There is also an integral cassette interface, software and hardware, using named cassette files for data and program storage, enabling more than one program to be stored easily on each cassette.

**DATA TRANSFER RATE:** Tape 300/1200 baud, VDU equivalent to 5K Baud with auto paging.

**HARDWARE AVAILABLE:** Options include cassette, single or dual mini–floppy discs, dual double–sided eight inch discs (1MB), serial, parallel and analogue interfaces, printer.



# computing today

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P.O. Box 79,
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**Our parent magazine, ETI, has published details of a game called 'AMBUSH!'. Here Pete Howells presents a version written for the PET computer.**

In attempting to reproduce the game on a PET a number of restrictions must be accepted unless specific hardware add–ons are built. Firstly the lack of sound effects. The ETI game uses a number of different sounds for 'attack', 'hit', 'fire' etc. On the PET these must be replaced with written messages or graphics effects. Secondly the lack of colour. Nothing can be done about this unless you are prepared to colour specific areas of the screen like some pub and arcade games. Finally, simulating the effect of holding down one or more of the 'fire' buttons. On the ETI game ammunition is consumed all the time that a 'fire' button is held down. Using the GET command in PET BASIC will input one character from the keyboard buffer and holding down a key will not cause a stream of characters to be entered. The only way round this is to only allow enough ammunition to complete the game. This means that any attempts to predict the course of the attack will waste ammunition and you will lose the game.

**Setting 'em Up**

```
10 DIM M(4,3)
11 DATA 32793,0,+80,33205,0,-2,33753,0,-80,
                                 33181,0,+2
12 FOR I=1 TO 4
13 FOR J=1 TO 3
14 READ M(I,J)
15 NEXT J
16 NEXT I
20 INPUT "3SET SPEED (1 TO 9)";S
21 IF S<1 OR S>9 GOTO 20
22 SS=INT(100/S)
```

The array 'M' is a table of starting position and directions of movement for attacks, an extra store is provided to record the current position during an attack. The table is set up in the double loop in lines 12–16, using the data at line 11. The speed at which the game is played is input and set in lines 20–22. 'SS' is the value used in a delay loop further into the program. The character '3' in line 20 is the printers interpretation of a 'CLEAR SCREEN' character (SHIFT/CLR-HOME), and should be entered as such when typing in the program. (This occurs in a number of places in the listing where cursor control characters and graphics characters are used. Graphics characters are reproduced as the lower case letter of the key on which they appear.)

**Playfield Display**

```
39 PRINT "3"
40 PRINT "AMMUNITION                 w"
41 PRINT "INDICATOR"
42 PRINT "q 100                      w"
43 PRINT "q"
44 PRINT "q 80                       w"
45 PRINT "q"
```

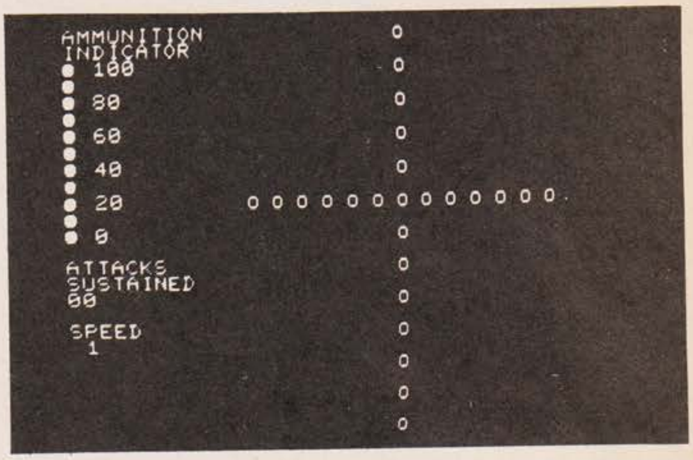



Figure 1. The display at the start of the game.

```
46 PRINT "q 60                     w"
47 PRINT "q"
48 PRINT "q 40                     w"
49 PRINT "q"
50 PRINT "q 20          w w w w w w w w w w w w
                                          w w"
51 PRINT "q"
52 PRINT "q 0                      w"
53 PRINT
54 PRINT "ATTACKS                  w"
55 PRINT "SUSTAINED"
56 PRINT "00                       w"
57 PRINT
58 PRINT "SPEED                    w"
59 PRINT S
60 PRINT "                         w"
61 PRINT
62 PRINT "                         w"
63 PRINT
64 PRINT "                         w";
```

Lines 39–64 print the game display on the screen. Again the '3' at line 39 is a SHIFT/CLR-HOME, and the 'q' and 'w' are the equivalent graphics character. The semi–colon at the end of line 64 is necessary to prevent losing the top line of the display as the cursor returns to the start of a new line after having written the entire screen.

**Counting It Up**

```
70 H=0
71 AA=0
```

Lines 70 and 71 initialise the two counters, 'H' for attacks sustained and 'AA' for ammunition used.

**To Attack Or Not To Attack?**

```
100 IF RND(TI) >.994 GOTO 115
110 GOTO 100
```

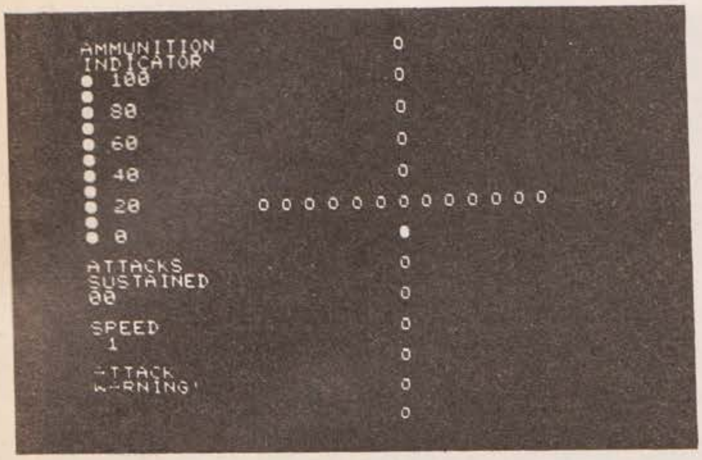



Figure 2. An attacker approaches from behind.

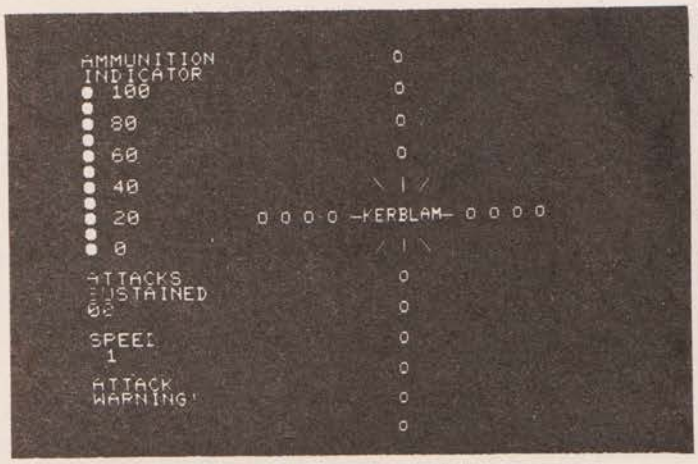



Figure 3. Tha attacker reaches his target and the game is lost.

```
115 AX=0
120 X=RND(TI)
130 IF X<=.25 THEN D=1
140 IF X>.25 AND X<=.5 THEN D=2
150 IF X>.5 AND X<=.75 THEN D=3
160 IF X>=.75 THEN D=4
200 POKE M(D,1),81
205 IF D>1 THEN PRINT "ATTACK======
                            WARNING!";
210 M(D,2)=M(D,1)
```

Lines 100 and 110 introduce a suitable random delay between attacks by looping until a high enough value is taken. The value of .994 causes an average delay of about 2–5 seconds, but the actual delay may be anything from zero to just short of infinite! AX (line 115) stores the direction of fire and is reset to zero from the previous direction. Having decided to initiate an attack a direction is chosen, again through the RND function, and D is given a value corresponding to this (1-4, clockwise from the top). The approaching attacker is then POKED into position on the display with reference to table M. Note that in line 205 the exact sequence of characters within the quotes is HOME, 21 occurences of CURSOR DOWN, 'ATTACK', CURSOR DOWN, 6 occurences of CURSOR LEFT, and 'WARNING!'.

**...Nobler Of The Mind To Bear The Slings And Arrows Of Outrageous Computer Games...**

```
215 IF AA=100 GOTO 276
220 GET A$
225 IF A$="" GOTO 276
230 IF A$="8" THEN AX=1
240 IF A$="6" THEN AX=2
250 IF A$="2" THEN AX=3
260 IF A$="4" THEN AX=4
```

If you've already used 100 shots then you can't fire anymore and are thus rather out of luck! If you can you use the the keys '2','4','6' or '8' on the keypad to indicate the direction you wish to fire in. AX is set to this direction in the same manner as D in lines 130–160.

**A Shot In The Locker?**

```
261 AA=AA+1
264 PRINT ""
265 FOR AB=1 TO 1+INT(AA/10):PRINT "";:NEXT
                                        AB
266 PRINT "w";
```

The ammunition counter, AA, is incremented. The ammunition indicator on the screen is decremented in steps of 10. Line 246 contains the HOME character between the quotes. The cursor is then moved down the indicator scale, once for each 10 shots, and a new character printed over to give the impression of lights going out on the scale.

**Hit, Miss Or Dead!**

```
275 IF AX=D GOTO 500
276 IF M(D,2)=33193 GOTO 600
278 POKE M(D,2),87
280 POKE M(D,2)+M(D,3),81
290 M(D,2)=M(D,2)+M(D,3)
300 FORSA=1TOSS:NEXTSA
320 GOTO 220
```

Line 275 tests if the attacker has been destroyed. Line 276 tests if the player has been destroyed. M(D,2) is the current position of the attacker, 33193 is the position of the player at the centre of the display. Lines 278–290 first POKE a blank to the current position of the attacker on the screen, alter the current position according to the direction of travel, and POKE the attacker into the next position. Line 300 then provides the speed delay.

**Hit!**

```
500 POKE M(D,2),42
510 H=H+1
```

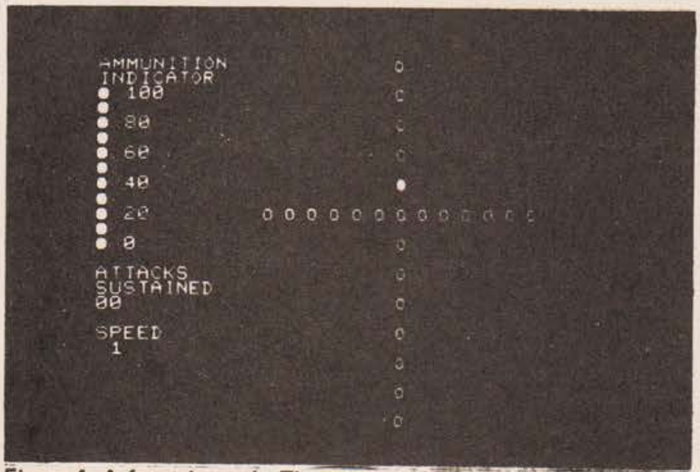



Figure 4. A frontal attack. The message 'ATTACK WARNING!' does not appear.

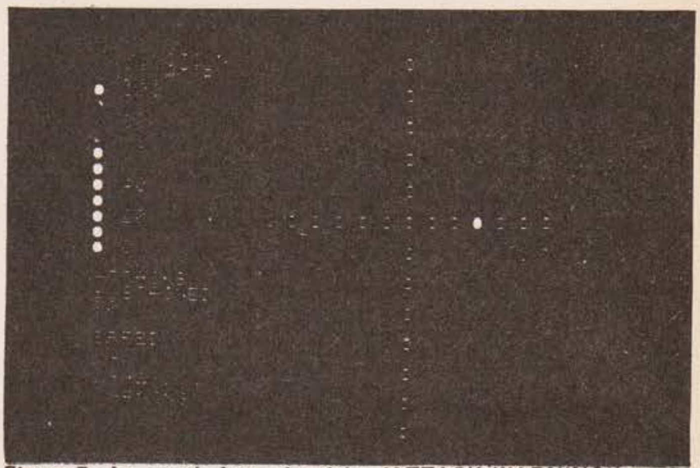


Figure 5. An attack from the right. 'ATTACK WARNING!' can be seen at the bottom left of the screen.

```
520 PRINT "";H;
525 POKE M(D,2),87
527 IF H=100 GOTO 900
528 PRINT "        ======          ";
530 GOTO 100
```

A minor explosion is POKED to the position of the attacker, the attacks sustained counter is incremented and the screen display updated, the explosion is cleared from the screen ready for the next attack. The characters within quotes on Line 520 are HOME and 16 occurences of CURSOR DOWN.

**Miss!**

```
600 POKE 33190,11:POKE 33191,5:
     POKE 33192,18:POKE 33193,2:POKE 33194,12
610 POKE 33195,1:POKE 33196,13
612 POKE 33111,77:POKE 33113,93:
                 POKE 33115,78:POKE 33189,64
613 POKE 33197,64:POKE 33271,78:
                 POKE 33273,93:POKE 33275,77
615 FORXX=1TO1000:NEXTXX
620 GOTO 20
```

The attacker has reached his target and the player is wiped out. A 'KERBLAM' explosion is displayed on the screen, held for a while, and the game restarted.

**Success!**

```
900 FOR I=1 TO 500:NEXT I
905 PRINT "3CONGRATULATIONS! - YOU HAVE WIPED
                                         OUT"
910 PRINT "THE ENTIRE YAPPANIE SUICIDE SQUAD
                                         AND"
920 PRINT "SAVED THE CEETEE FROM DESTRUCTION"
930 PRINT
940 PRINT "ARE YOU FEELING FIT ENOUGH FOR"
950 PRINT "ANOTHER MISSION?";
960 GET A$
965 IF A$="" GOTO 960
970 IF A$="Y" GOTO 39
980 STOP
```

A congratulatory message is printed on the screen, (again the 3 is SHIFT/CLR-HOME), and the game either restarts from scratch or is stopped according to the players response.

**Run—Out**

This game has been written specifically for the PET. If you want to adapt it for another machine (which must employ a memory mapped VDU, as it is for this form of display that the logical structure has been written ) you will probably need to use the graphics and cursor control characters specific to that machine. You will also need to modify all the values given for screen locations, mostly in array M, but that's your problem.

Our thanks to the Byte Shop at 48 Tottenham Court Road, London W1 for the use of their printer to produce the listing in this article.

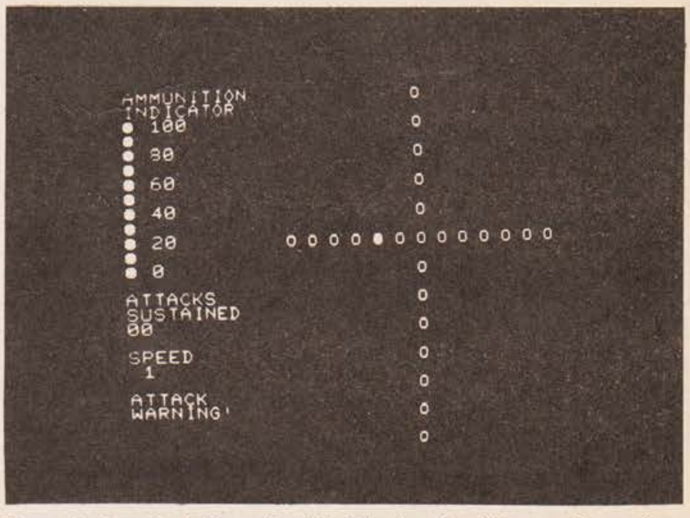


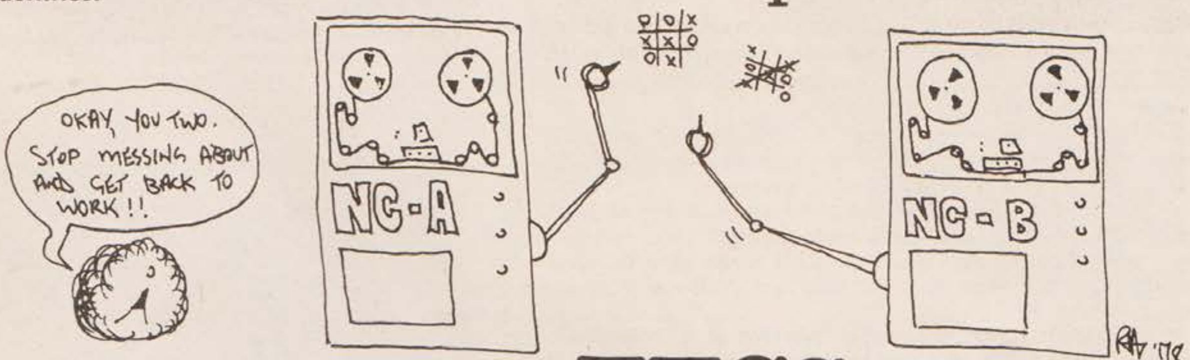

Figure 6. An attack from the left. The length of the warning varies — less from the front, longest from behind, and, in addition the message 'ATTACK WARNING!' appears for all but frontal attacks.

# computing today

## MAY ISSUE On Sale April 20th

# Softspot Special

A selection of readers programs for you to try out on your own machines.

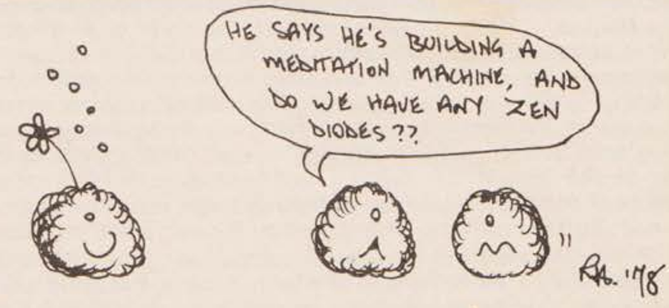



# TECS System

We reveiw a new British home computer that features a full Teletext system built in as well as having all the usual expansion facilities.

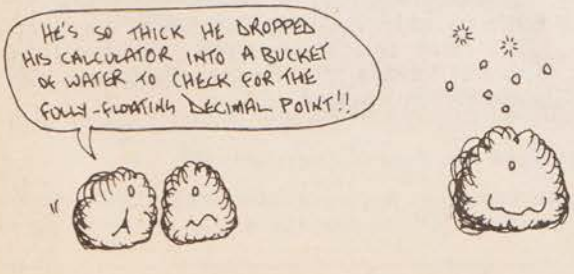
# Word Processor Survey

Fed up with all that typing? We take a look at the Word Processor programs available for your home or office computer system.




# S100 16K RAM

If you need more memory we can help you. This month's project is a 16K expansion for the S100 bus.



**By Gerald Chevin:**

The annual trek to the Winter Consumer Electronic Show (WCES) Las Vegas, Nevada, really proved to be a Star Trek; the enterprise in this case was the sheer inventiveness of electronic wizardry applied to all the facets of the industry.

This years show dwarfted last years gathering with 811 exhibitors, more than 40,000 attendees and almost 500,000 sq. ft. of exhibit area. Also, unlike last years show which was dominated by home computers, a complete across–the–board outpouring of new products in various categories like telephones, televisions, programmable video games, video disc players, compact audio components, pre–recorded video tapes, security systems, mobile stereo and hand held games occured.

### New TV Systems Launch

A great deal of attention was focussed on units termed 'min–icombos' which feature a small screen monochrome televis–ion, am and fm radio and an audio cassette deck packed into one hand–held lightweight unit.

JVC are posing a threat to the Sinclair Microvision with their "TWINCH" 2" T.V. receivier which weighs a mere 2.42 pounds and includes fm, am sound.

At the other end of the scale, large screen projection television units were evident from General Electric relaying the local channel 10 Television CES News in a number of selected areas. Also in this field are National Panasonic, Sony and Advent.

One of the more novel systems was displayed by Hitachi, a dual TV picture, or picture in a picture display. Unlike most European entries into this field, the Hitachi remote controller allows the inserted picture position to be determined by the viewer, it also permits "freezing" the inset picture which incidently is in colour.

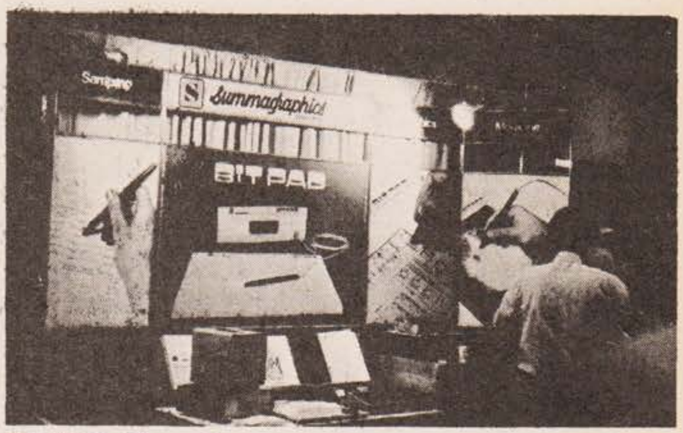
There are two approaches to be considered for this feature, Fairchild Camera and Instrument Corporation uses charge coupled devices to store the inset picture in an analogue format, the other by Hitachi uses a digital memory. The Fairchild system is more conventional using two memories, one for each inter–laced field of the inset picture, whilst one memory is storing one 120 element by 80 line field, the other memory is reading out the previous one.

The monochrome inset is 1/3 of the scale or 1/9 of the area of a large picture. The system uses charged coupled devices to store the inset rather than bucket brigade devices because the signal loss of the latter can cause a weak or snowy picture. Both memories are in one chip another innovation. Hitachi use of digital memory is extracted from standard broadcast technique without the frightening expense. To achieve this end they employ line sequential coding which is based on the high correlation between successive TV fields i.e. there is relatively little change from one to the next. This method allows all luminance data to be stored in one 64–line by –96–element by 5 Bit per element memory, and read out three times faster through a small buffer memory that prevents a read write conflict.

A 96 element horizontal resolution gives the inset picture with 1/14th the area of a large picture, the same band width as a large one but the inset resolution is lower but adequate for its size. Colour data for every other inset picture is stored in a separate 64 line by 48 element by 5 bit digital memory. A one chip 4 bit microprocesser controls the system.

### Expansion Of The Home Video Market

Another upgraded item shown was the second generation of home video recorders. The National Panasonic VHS home video cassette recorder is based around a microprocesser timer, it will allow you to automatically record four diff–erent TV shows at different times and on different channels for one week in advance; it also features an automatic




**The Bit Pad is a rather nice (but expensive) device for turning freehand into computer input.**

**Software for the TRS 80 was available from many suppliers. This stand is demonstrating a chess recorder program.**

television/VCR switch to flip to the TV mode when the power is removed.

A tremendous library of video tapes including such exotic titles as "Erotikus","A Dirty Western" and "X–rated cartoons" are flooding the consumer market from numerous companies in the US.

The video disc war is now hotting up with Phillips subsidiary Magnavox launching its Magnavision with an initial two hundred Discovision catalogue by MCA. This machine is based upon the laser beam technology whilst RCA Selectavision is supposedly starting with two hundred and fifty titles ranging from from feature films to do–it–yourself discs. The RCA system is based upon a capacitance pick–up and this technology should result in a price tag about three hundred dollars less then the Magnavox system, Magnavox plan approximately 20,000 players for the first year and Magnavision player uses two kinds of 12" discs, the 30 minute per side record spinning at a constant 1800 revolutions per minute and the 60 minute per side playing back variable angular volocity information is stored in the pits burned into the disc by a laser during manufacture. The pits patterns contain the analogue representations of the picture and should read out by helium neon laser, the records are made by MCA a Phillips partner in developing the player. The other companies working on laser based play back systems include the French Thompson CSF Group and Japans Hitachi Limited.

### Diversification In The Home Computer Field

In the home computer market a reported 240,000 mach–ines were sold in 1978 in the US and a projected figure

# WCE SHOW REPORT

**Against a background of arcade machines the young American public gaze at a model train layout, microprocessor controlled of course!**

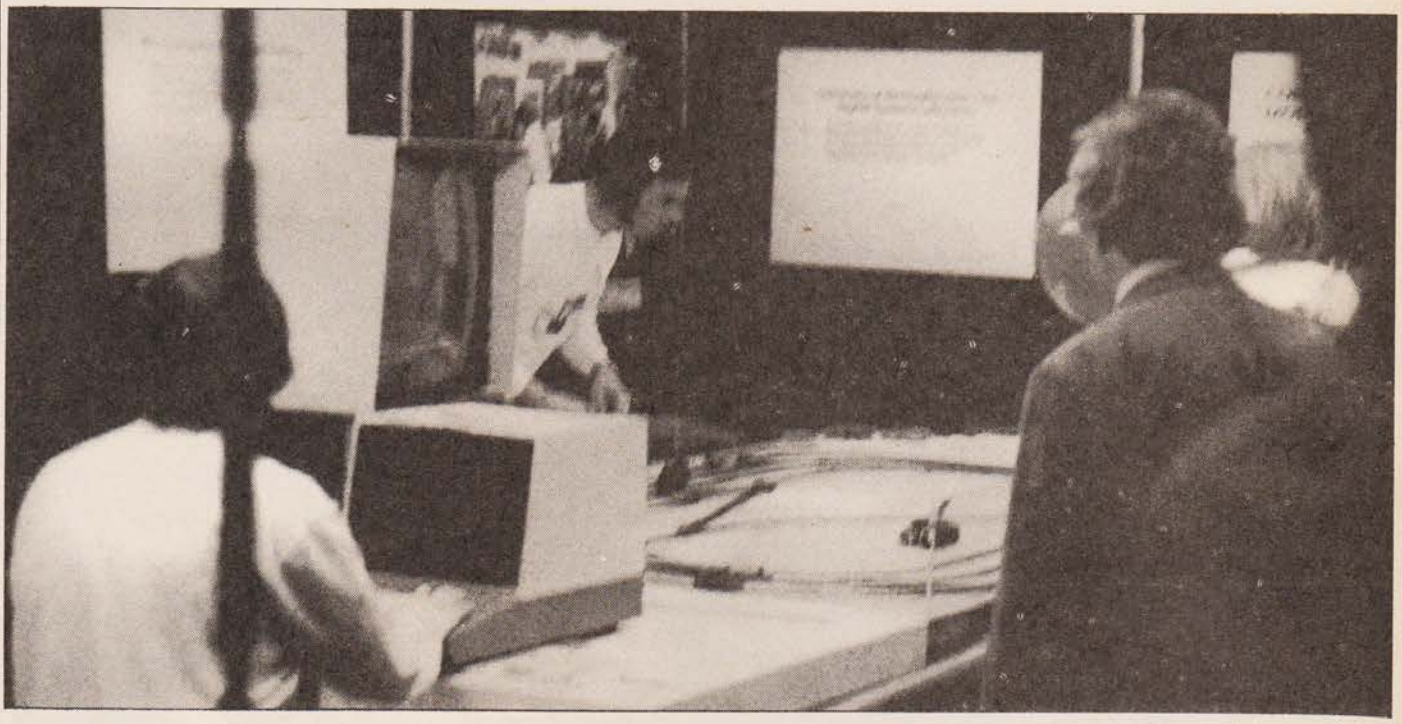
of 400,000 is expected for 1979. In this light Atari Inc., a division of Warner Communications have released two home computers, the 400 system and the more expensive 800 system. A brief description of each is listed below. 400 unit central processing unit uses 6502 chip, the Random access memory contains 8 000 bytes,the Read only memory is expandable from 8,000 to 16,000 bytes by using stored solid state cartridge programmes, colourgraphic in 16 colours with 8 luminance levels. The educational library of pre–recorded software on ROM contains more than 70 hours of instruction in over 20 subjects including Algebra, Spelling, Auto–Mechanics, Spanish, Great Classics, US History, Basic Electricity, Carpentry, Zoology. The 800 system, however, has a lot more memory capacity and will operate for example a four disc memory, printer, cassette acoustic modem, light pen, voice sythesis and music synthesiser. It's ready shipped with 8 000 bytes of RAM which is expandable to 48 000 bytes of RAM and may be applied to some of the following purposes. Personal Financial Management Income and Expense Records, Mailing Lists, Computerised Appointment Calendar, Payable Accounts etc., A major innovation with this system is the availability of a data cassette with an audio track to inform via your receivers loud speaker, whilst the data track draws graphics and writes on the TV display.

### We Speak Your Language

Not to be out–done by the competition the Bally Corporat–ion take the view that few people will actively want to program their home computers and have introduced a new language that uses words instead of letter number confiurations to make it seem friendlier. It was devised from the computer language used to create special computer effects in the film "Star Wars", it is called GRAFIX, de-veloped by Tom Defanti Professor of Computer Sciences of the University of Illinois. For example when the user is uncertain of his or her next move in the programming sequence they just type in "help" and the computer responds with a sequence of directives which show the proper method.

The Video Console has already been available in the USA for some time with the addition of the keyboard and software cassettes which should be ready by the Summer of 1979, a fully fledged easy to use computer at only 900 dollars is well within most of the American publics reach.

The expected introduction by Texas Instruments of a home computer did not materialise, we did however see a number of voice orientated products, Texas Instruments, "Speak and Spell" now has one extra plug–in module termed "Vowel Power", it costs about 15 dollars and stores about 140 words on one 128K Rom, unfortunately there is a pronounced Texan accent on the original module, and the newcomer; but I was assured that an English (as opposed to an American) module is under development. The famous Chess Challenger narrates each move via a multi–chip speech synthesiser and should retail for only 325 dollars in the summer. A new device is now on the market called the Hand Held Language Translator. One is manufactured by the Craig Corporation in California, the other is by the Lexicon Corporation, Miami, Florida. Both units store words and phrases in English, and other languages and display a trans–lation from one language to another after a word or phrase is keyed in. Both use an 8 bit 3870 micro–computer from Mostek and plug in function or language modules having a 1500 word vocabulary. Further both machines are different and this affects the price. Craig puts its micro–processer into the keyboard unit, its memory into the plug–in module, Lexicon on the other hand use the keyboard unit as a general



purpose interface, both memory and the micro–processer are in the module according to Lexicon the hand held device is thus suited to a far greater variety of functions, some not even developed yet!

### Electronic Games Run Riot

Apart from the Fidelity Chess Chalanger already mentioned above there was a big shift in this show towards non–TV based hand held games by a large number of manu–facturers including Coleco, Mattel, Chafitz and Tryom. Mattel's entries include the following:

'Horoscope Computer' with a 'Valid' astrological calculater (three years from the 3lst May 1979). There are read out activation keys for the following areas:–love, Money, Career, Friends, Family, Sport and Creativity! Armour Battles, Sub–chase, Football and Hockey are self–evident. Unlike "Battle Star Galactica Space Alert" in which the cyclon raiders land and relaunch their attacks indicated by blips of LED light moving toward the battle star. You arm your laser torpedo to intercept. Naturally all the events are also fed via a sound processer chip to a loud speaker.

The Coleco range includes a quick response challenge called "Zap"! and "Amazatron" is designed to generate musical notes, rasberries or fan fares depending on your direction finding abilities. "Boris" by Chafitz the other computer chess game had produced a variety of "Limited editions" destined to become pieces of furniture with a built–in computer. They have also developed a portable battery operated unit termed "Boris Master" and another first "Boris Grand Master" where it will actually "move" its own pieces! which are in reality a comprehensive electronic display.

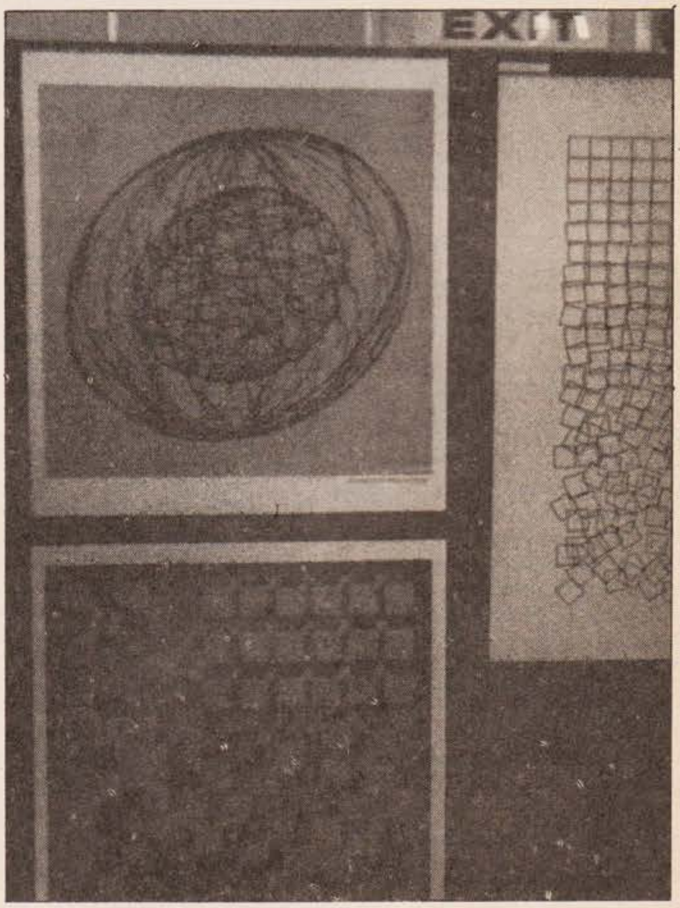
Finally . . .

Tryon Inc., showed their "Omar" range. "Omar III" is capable of playing a highly sophisticated Backgammon game with any existing board or with its highly attractive tournament size board. You guessed it, it is also a portable device with a distinctive LCD display which also includes a "pip" count calculator and a selection of either classical or modern play.

This along with many of the other products will not be available until the summer which is also the time for the Summer CES Show and another Star Trek for yours truly.

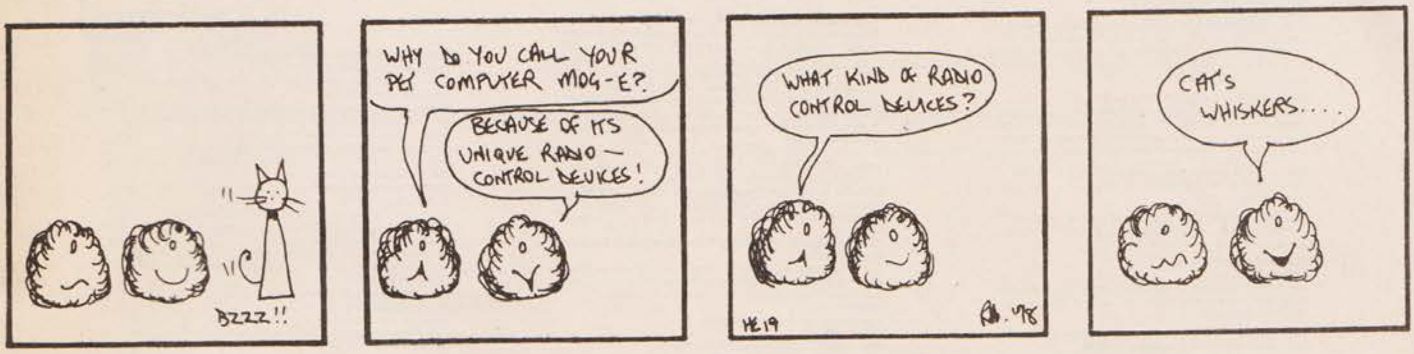
**Yet another microprocessor controlled train set in action, the control being handled from a Newbury terminal.**

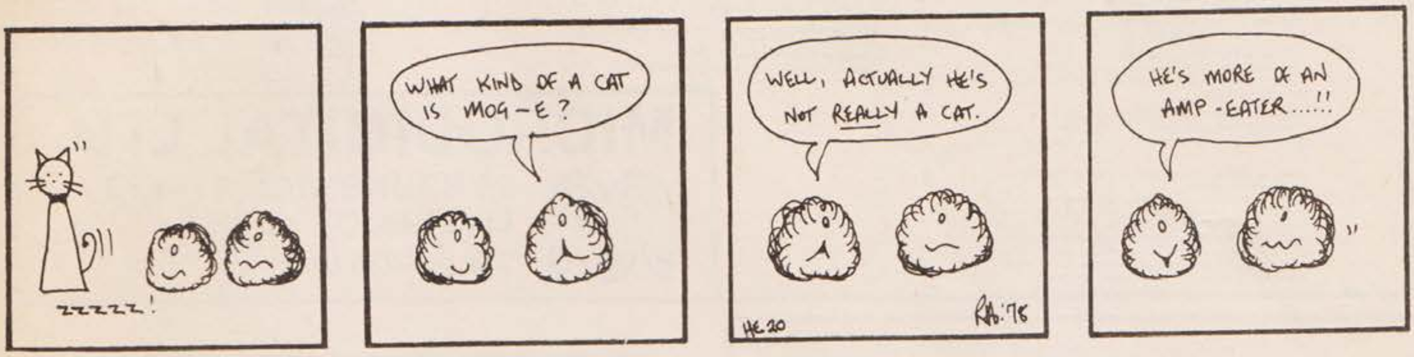
**A display of some of the computer art that was on show at WCES.**

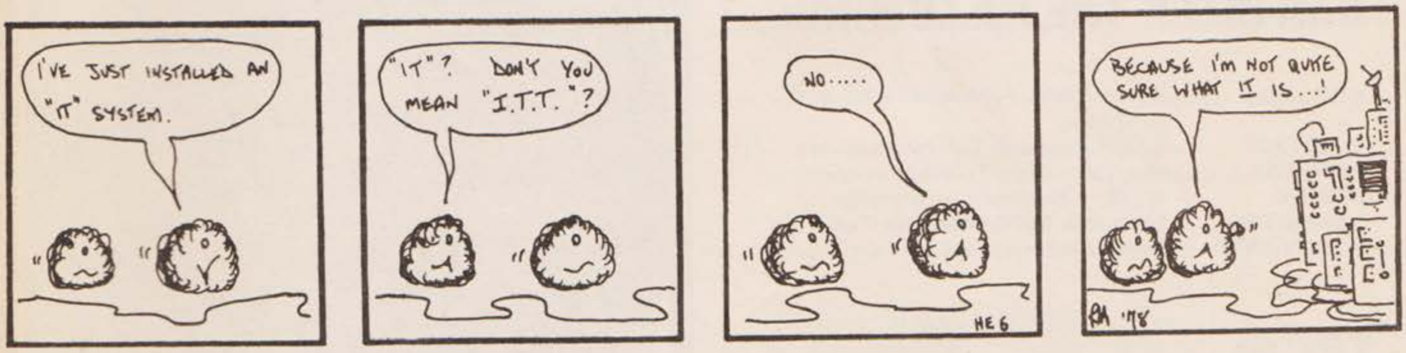



*Should you be interested in any of the above products please contact myself via CT and we will endeavour to inform the distributors of your interest.*

# BEASTIES






RA. '78

# DATA SHEET

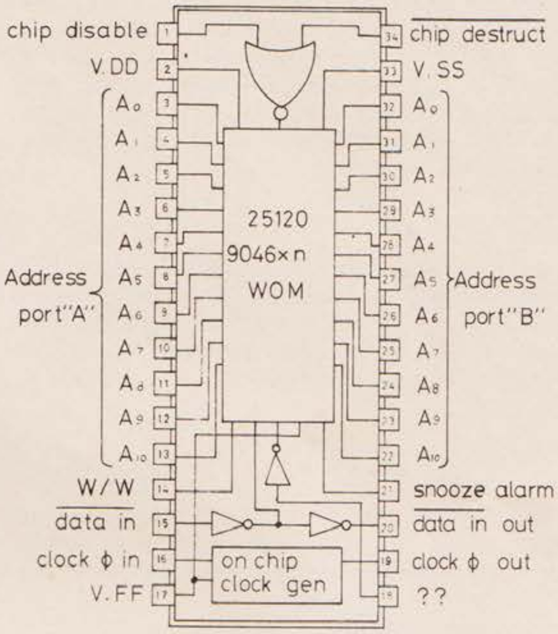
**PNMOS**
**LSI**

**TYPE 25120**
**9046×n BIT RANDOM ACCESS WRITE ONLY MEMORY**

revised april 1984

## applications :

- least significant control memories.
- post mortem memories.
  (weapon guidance systems)
- artificial memory systems.
- non-intelligent micro controllers
- first-in never-out (FINO) asynchronus buffers.
- overflow register (bit bucket.)




## features :

- fully encoded multi-port addressing.
- write cycle time 79ns (max typ).
- read access time[1]
- cell refresh time 2ms (min typ).
- TTL/DTL compatible inputs
- clock input capacitance 2pF max[2]
- V.DD = 0v ± 3%, V.CC = 10v, V.FF = 6,3v AC.

## description :

The 25120 is a 9046×n bit random access write only memory Due to the employment of our proprietary Sanderson-Rabbet enhanced depetion mode which utilises both P & N channel M.O.S devices the 25120 is capable of 50% higher speeds than you will be able to obtain. A single TTL level clock phase is required to drive the internal clock generator. The static memory cells are operated dynamically to yield an extremely low power dissipation providing the chip is properly cooled. This is easily done with a 6ft fan placed 1/2" from the package. If the device fails you have exceeded the ratings, under these circumstances a larger fan is recommended. All inputs and outputs are directly TTL compatible[3] providing the correct interfacing circuitry is employed. In any event use a 1A fuse in all supply and data lines.

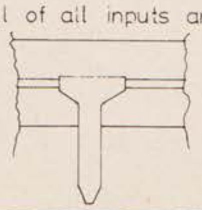
3

The use of the unique SEX[4] process allows phenomenal rates of production[5] thus ensuring the availability of this versatile device. All terminals are provided with slip-on latex protectors for the prevention of Voltage Destruction (pill packaged devices do not require protection.). The use of a low cost silicone DIP packaging ensures reliability by the use of non-hermetic sealing which prevents the capture of harmful ions while allowing the free exchange of friendly ions.

Data refresh is accomplished during CB[6] and LH[6] periods.

notes :-

1) not applicable.
2) measured at 1·3MHz with 26mV into 1·9pF.
3) we dont know how but you can take our word for it.
4) Special EXtra secret.
5) see modern production techniques by T. Arrieta (not yet written).
6) coffee break and lunch hour.
7) typical of all inputs and outputs.



S-149

A new interface module has been introduced in the UK by Petsoft to allow their CMC Word Processor pack–age to output hard copy onto any RS232 device. The unit plugs directly into the IEEE–488 bus port at the rear of the PET and is supplied with a modular power supply and all the necessary leads. Although the Baud rate is factory set 300 you may specify any rate between 110 and 9600 when ordering; To give greater flexibility to the user instructions are provided to enable you to adjust this at a later date. A DIL switch is mounted on the underside of the unit to enable the user to select the number of stop bits and also the type of parity and these facilities will allow almost any printer to be connected. As well as providing the output port for the Word Processor this interface may be used as a listing output or during programs.

### Installation

Actually connecting the unit is very simple. With the PET turned off you plug it into the IEEE–488 socket, that's the one nearest to the mains lead, and then turn the PET back on. Now all you have to do is connect the RS232 lead to your printer and plug the power supply module in and off you go.

### Calling It Up

To actually get anything out of the unit it must be called under software control. To use it under monitor to output a program listing you have to type the following commands:-

```
OPEN 5,5
CMD 5
LIST
```

If you want to get output during an actual program run you must treat the port as a file, to do this you have an instruction at the beginning of your program OPEN 5,5. At any time that you want the output to go to the printer rather than screen the instruction PRINT #5, before the output string will perform this. If you are running the CMC Word Processor package the printer is assumed to be the output port, via the module of course, unless you have previously patched the program.

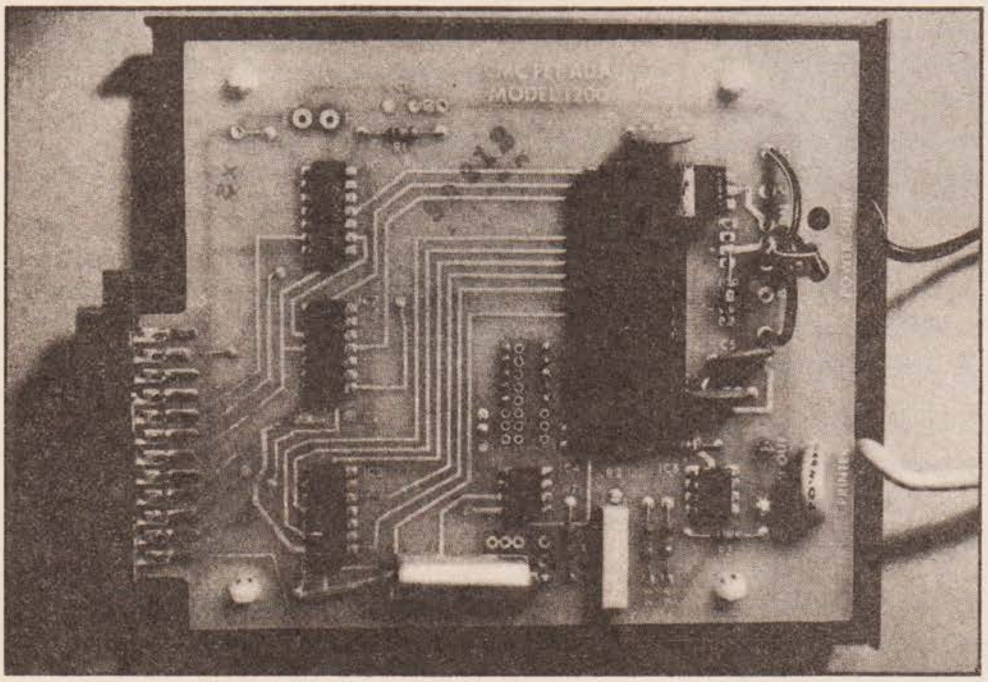
### The Inside Story

We had only one problem with the unit, our printer hadn't arrived, so we decided to take a look inside the case and see just what you'll get for your money. The circuitry is neatly laid out on one double–sided PCB which has plated through holes and is pre–tinned. The main IC is an MM5303, a UART so possibly a send and receive unit will be available soon. The clock is provided by a 555 and the rest of the chips are LS series TTL. The overall construction is good with everything being mounted on the board but the use of the PCB pillars as feet is a little suspect, one of ours was already broken off when we received the unit.

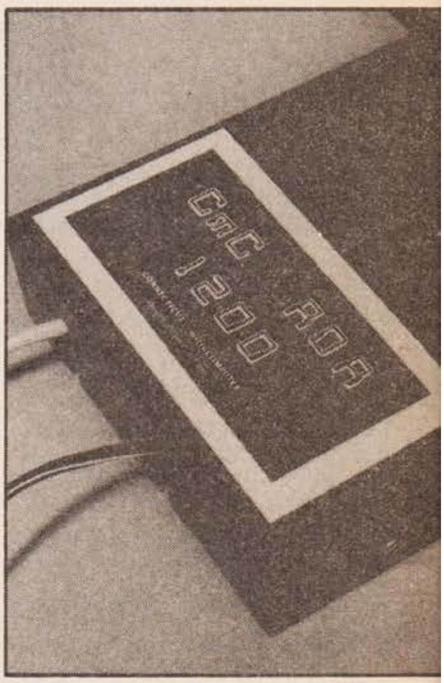
### Summary

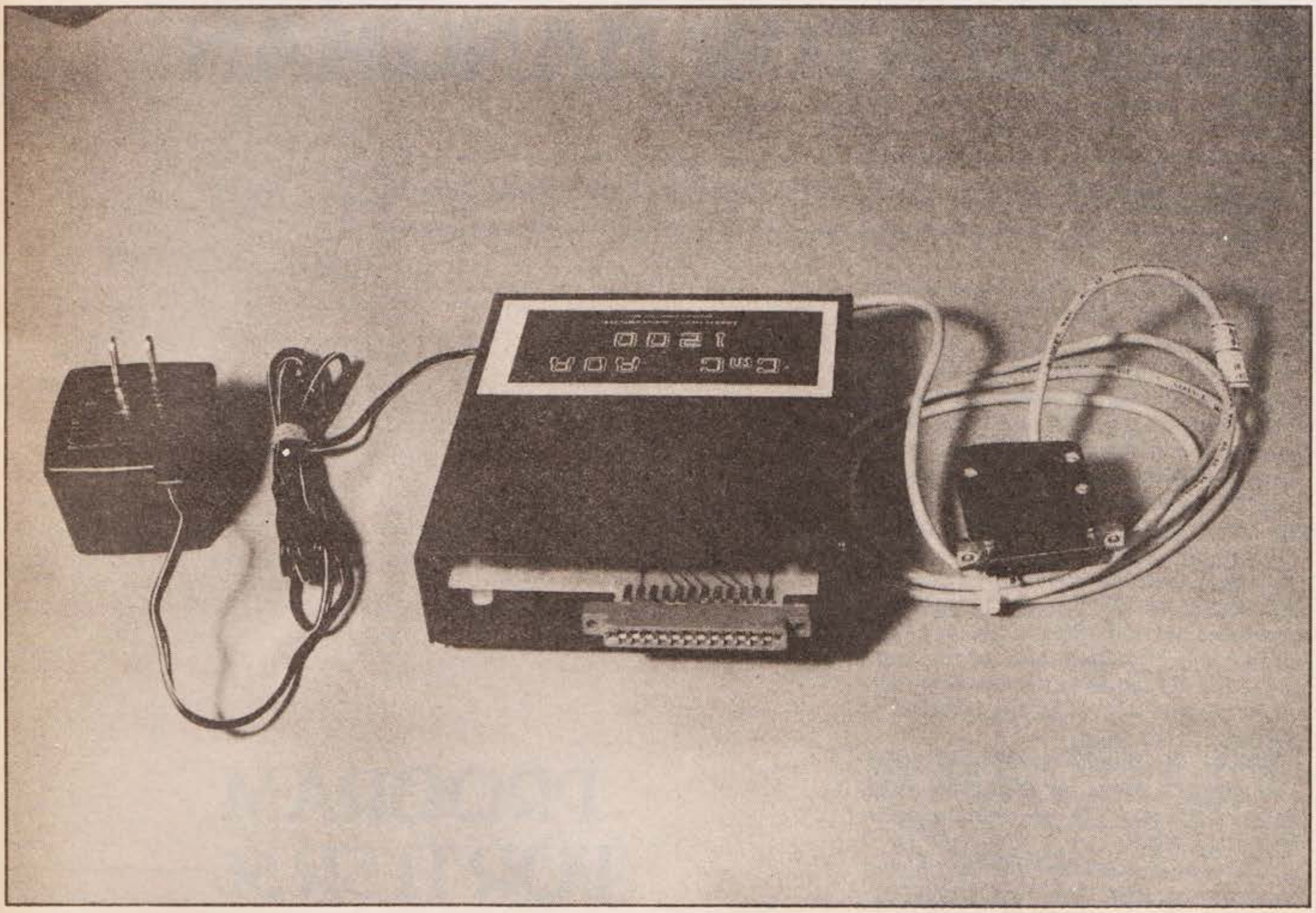
If you are considering a small word processing system based on the PET then the CMC package and this unit will provide for the needs of a small business or home system. The program will cost you £25 and the interface will set you back a further £90, the printer is obviously your own choice. The American price is S169 so the English price is quite reason–able and will allow you to go on–line to a printer, or even a modem rather quicker than waiting for Commodore. Many thanks to Julian Allason of Petsoft for allowing us to borrow the unit and program. A fuller report on the actual Word Processor program will be published in our survey in next months issue.

**An internal shot revealing the PCB and components.**



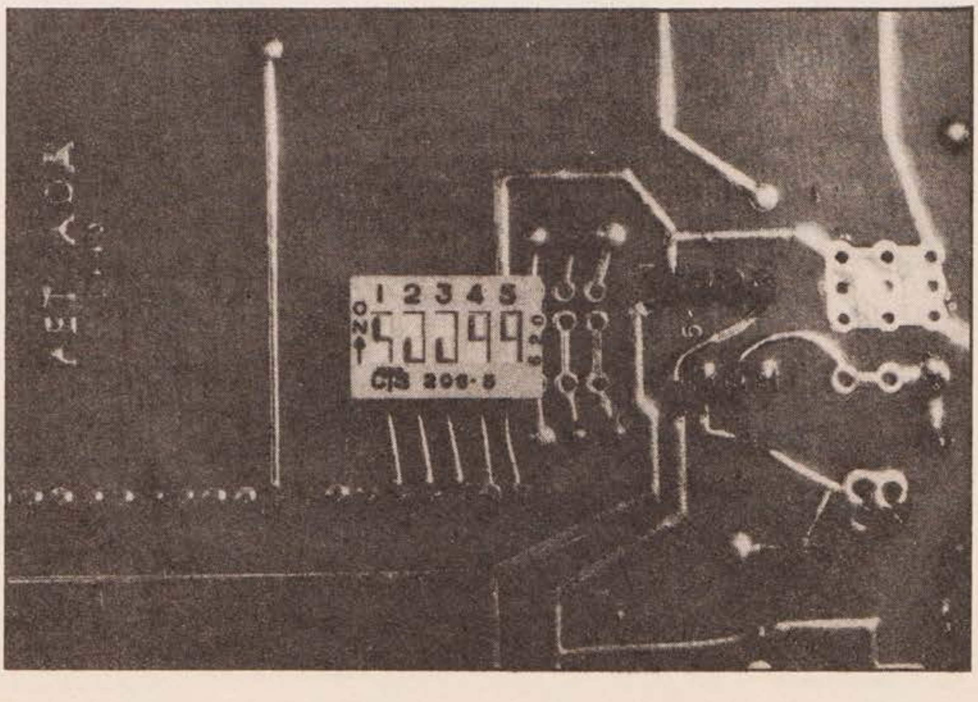
**The interface adaptor connected to our PET**





A general view of the unit with it's power supply and the RS232 lead.

The underside of the box showing the selection switch.



# CALCULATOR HANGMAN

Use your calculator for word games. By Rick Campbell of London Ontario.

THIS PROGRAM is a calculator version of the popular game "Hangman". The object of the game is to guess a hidden word which has been entered by your opponent. Guesses are made by entering a letter from the alphabet which the player believes is contained in the hidden word. Because calculators only accept numerical data the letters are represented by number combinations, with 00 being "A", up to 25 being "Z".

After a guess has been made a response will appear on the display. If the letter guessed is not contained in the word, the display will indicate a zero. If the letter guessed is contained in the word the calculator display will show the position of the letter in the word.

Example: The hidden word is "LOUD" The player's guess is "O" (14). The display indicates a 3, the third position from the right.

If the word contains more than one of the letters guessed, the display will indicate the position of all the correct letters.

Example: The hidden word is "STRUT". The guess is "T". The display will indicate a 41, fourth and first positions.

SAMPLE GAME

For TI SR 56.

Step 1. The word is selected and entered by the opponent. In this case we will use "TEST".

ENTER:
RST
19041819
R/S

Step 2. The word length is entered by the opponent.

ENTER:
4
R/S

Step 3. The player enters a guess.

The resulting game is shown in Fig. 1.

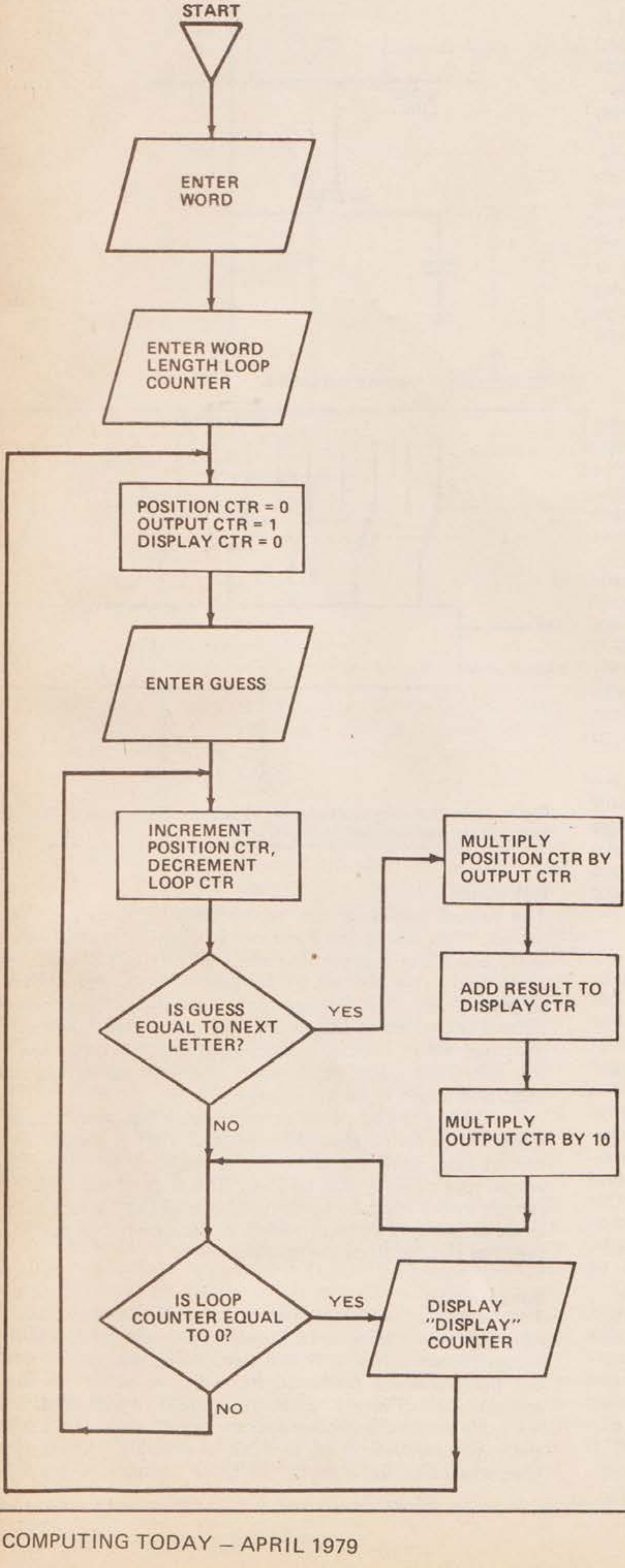
| ENTER | GUESS | DISPLAY | LETTERS USED | WORD |
|---|---|---|---|---|
| 00 R/S | A | 0 | A | **** |
| 04 R/S | E | 3 | AE | *E** |
| 08 R/S | I | 0 | AEI | *E** |
| 19 R/S | T | 41 | AEIT | TE*T |
| 18 R/S | S | 2 | AEITS | TEST |

*Fig. 1. Sample game.*

# PROGRAM FOR TI SR 56

| LOC | CODE | KEY |
|---|---|---|
| 00 | 38 | CMS |
| | 33 | STO |
| | 01 | 1 |
| | 33 | STO |
| | 02 | 2 |
| | 01 | 1 |
| | 33 | STC |
| | 05 | 5 |
| | 41 | R/S |
| | 33 | STO |
| 10 | 00 | 0 |
| | 33 | STO |
| | 03 | 3 |
| | 41 | R/S |
| | 54 | ÷ |
| | 01 | 1 |
| | 00 | 0 |
| | 00 | 0 |
| | 94 | = |
| | 32 | x ⇄ y |
| 20 | 01 | 1 |
| | 33 | STO |
| | 05 | 5 |
| | 00 | 5 |
| | 33 | STO |
| | 04 | 4 |
| | 33 | STO |
| | 06 | 6 |
| | 01 | 1 |
| | 35 | SUM |
| 30 | 04 | 4 |
| | 34 | RCL |
| | 01 | 1 |
| | 54 | ÷ |
| | 01 | 1 |
| | 00 | 0 |
| | 00 | 0 |
| | 94 | = |
| | 33 | STO |
| | 07 | 7 |
| 40 | 29 | INT |
| | 33 | STO |
| | 01 | 1 |
| | 34 | RCL |
| | 07 | 7 |
| | 12 | INV |
| | 29 | INT |
| | 12 | INV |
| | 37 | x = y |
| | 06 | 6 |
| 50 | 03 | 3 |
| | 01 | 1 |
| | 00 | 0 |
| | 30 | Prod |
| | 05 | 5 |
| | 34 | RCL |
| | 04 | 4 |
| | 64 | x |
| | 34 | RCL |
| | 05 | 5 |
| 60 | 94 | = |
| | 35 | SUM |
| | 06 | 6 |
| | 27 | dsz |
| | 02 | 2 |
| | 08 | 8 |
| | 34 | RCL |
| | 02 | 2 |
| | 33 | STO |
| | 01 | 1 |
| 70 | 34 | RCL |
| | 03 | 3 |
| | 33 | STO |
| | 00 | 0 |
| | 34 | RCL |
| | 06 | 6 |
| | 54 | ÷ |
| | 01 | 1 |
| | 00 | 0 |
| | 94 | = |
| 80 | 41 | R/S |
| | 22 | GTO |
| | 01 | 1 |
| | 04 | 4 |

# SOFTSPOT

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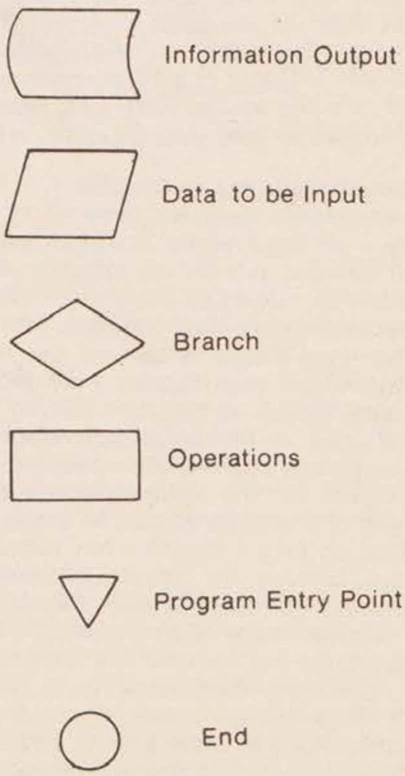


Now that single chip 16384 bit memories are readily available, even if still a little (I almost wrote bit) expensive, the possibility of using only eight chips to produce a 16K byte memory would seem to be a possibility. Even at the current price of £80 for eight devices this price compares favourably with the 128 devices required if IK static memories were used. Further price reductions are certain, as shown by the 4K memories which were similar price less than a year ago and are now available for around £2 each. Dynamic memories also have the advantage of power savings, and equivalent static memory array (128 x 2102's) would consume nearly six amps at five volts compared with the mere three tenths of an amp of the dynamic array. A dynamic memory can often be added without uprating the power supplies, this would obviously not be the case if IK static devices were used.

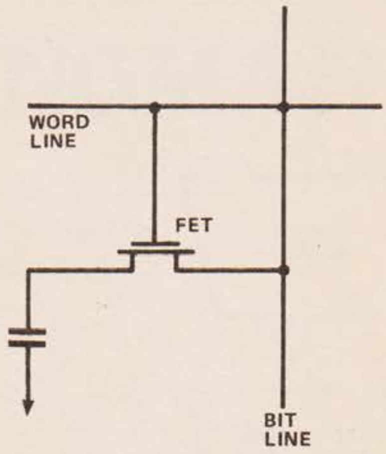



**Fig 1. A typical memory cell circuit.**

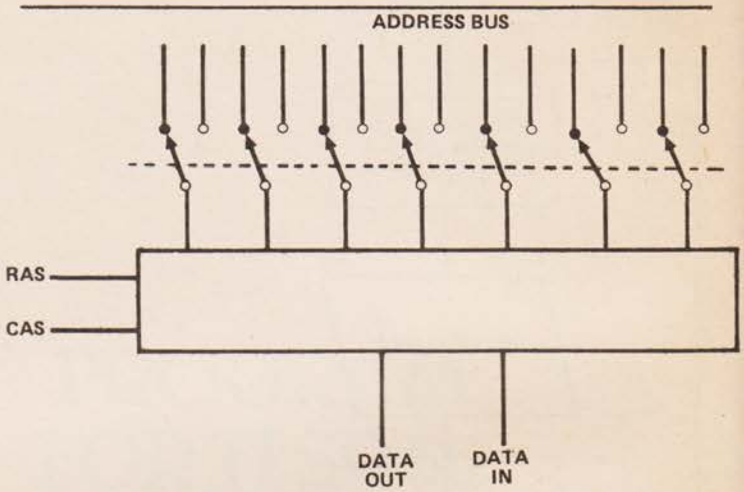



**Fig 2. How the chip multiplexes 14 address lines onto 7 pins. The switches are incorporated in the IC itself.**

### Advantages And Disadvantages

If dynamic memories have these obvious advantages why are they not used more widely. The answer is that there are disadvantages as well. To understand how these disadvantages arise the way in which dynamic memories function requires some explanation. In a modern device each storage cell consists of a single MOS transistor and a capacitor (Figure 1), whether the capacitor is charged or discharged indicates whether the bit is a '1' or a '0'. The charge on the capacitor gradually leaks away and must be topped up or refreshed at regular intervals. Additional circuitry must therefore be used to ensure that each storage cell is refreshed at least every 2 mS, this may be effected either by a normal read or write cycle or a special refresh cycle which does not enable the chip. Also, until recently, dynamic memories required special high voltage (12V) circuitry to drive the clock inputs (chip enable).

Overall the added complexity of the refresh circuitry means that unless large memory arrays are being built it is far easier to use static devices. The 16K bit dynamic RAM now makes this effort well worth while. These devices are only available in a 16 pin package and all inputs and outputs are compatible with TTL levels so that standard TTL chips can be used throughout the refresh circuitry.

### Squeezing A Quart Into A Pint Pot

Fourteen address lines are required to access 16384 bits, four pins are required for power supplies, two pins to get data in and out and one to indicate whether data is to be read from or written to the device. This makes a total of 21 lines,so how are they squeezed into a 16 pin package? The ingenious answer is to split the 14 address lines into two sets which then require only seven pins. The first seven bits, known as the row address, are stored internally by a signal on the row address strobe (RAS). The remaining seven bits can then be applied to the same pins and again stored by the column address strobe (CAS). This switching or multiplexing of the address lines adds further complication to the circuitry but not as much as might be expected because the refresh addresses also have to be multiplexed onto the same pins. (See Fig.2.).

One advantage of this arrangement is that similar pin configurations can be used for the 4K, 16K and even the much publicised 64K memories.. The last of these only used a single voltage power supply and therefore has two spare pins for the extra address bits. Motorola's version even has provision for automatic refreshing which would eliminate this major disadvantage if you can afford a set of eight at around £80 each.

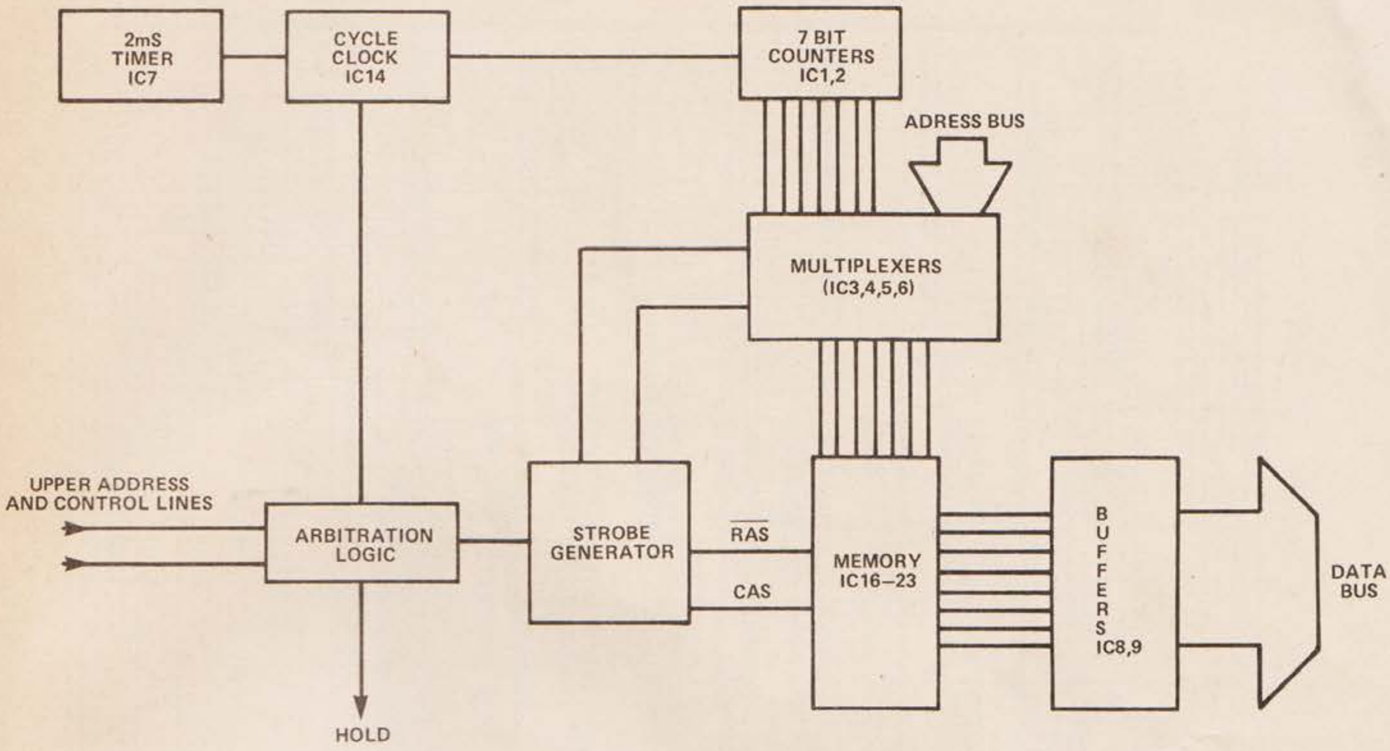
### Refreshing

The refresh sequence can be carried out in one of three modes. The first is the burst mode in which normal read or write operation is prevented while all of the 128 combinations of the row address are accessed. The second method is to periodically steal a single cycle from the microprocessor's normal operation to refresh a single row. The third method does not affect normal operation of the microprocessor as the refreshing takes place when the memory is not being used, and is said to be transparent.

Once a refresh, read or write cycle has been started it must not be terminated prematurely. That is another cycle cannot start until the current one has finished otherwise a whole row of data will be lost. This means that either the refresh cycles must be synchronised with the microprocessor clock or logic must be provided to decide whether sufficient time has elapsed since the previous cycle.

### Construction

The layout of dynamic memory boards can be critical as nearly all the power is consumed when the CAS and RAS inputs change state. Efficient decoupling is a must to prevent the transients produced from causing some interesting and unexpected errors. Each chip should be decoupled by at least one ceramic capacitor and the power supply lines especially ground should be as thick as possible. Other signal lines should be kept short. If these precautions are taken




A block diagram of the memory system.

veroboard can be used to produce prototype boards but a double sided printed circuit board is highly recommended, and a prototype PCB is shown in Fig.4.

**Memory Operation**

Outside the burst refresh period the output of the most significant bit of counter IC2 remains high and inhibits the oscillator formed by IC 14 c,d by forcing the output of IC 14c high. When a valid read or write signal occurs the output of IC 12c also goes high. This pulse appears in its inverted form at the output of 14a which in turn enables either the input buffer IC8 or the output buffer IC9 and, after the delay imposed by the RC network and IC 11e, produces a negative going pulse (RAS). This latches the row address supplied by the multiplexers IC3-6. After a short delay produced by IC 13b and IC 10b the multiplexer is switched to the upper seven address bits (column address). The column address is latched into the RAM by the slightly later pulse delayed by IC 13c and IC 10a. The relative timing of these pulses is shown in the figure. At the end of the access period the data is written to or read from the data bus via the buffers IC 8/9. Every 2 mS this process is interrupted by the 10 uS pulse produced by the astable multivibrator formed around IC7. This resets the counters ICl and 2 unless a read or write cycle is in progress in which case the counters are reset only when the cycle is completed. As a result the most significant bit output of IC2 goes low which in turn inhibits the production of the CAS pulses (IC 10a/b), starts the oscillator (IC14 c/d) and produces a hold signal to halt the microprocessor only if it attempts to access the memory during the refresh period (IC 12b, 11f). It also switches the multiplexer from the address bus to the output of the counters ICl/2. The oscillator output provides the clock for the counters and is also delayed by IC 11b, 13a, 14b, 11c to provide the RAS pulse for refreshing the memory. Thus each

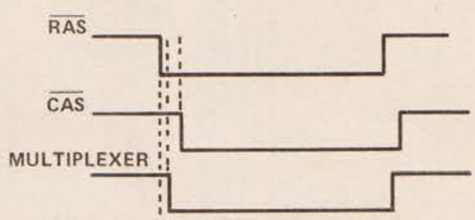



Fig 3. Typical waveforms of the row and column address strobes.

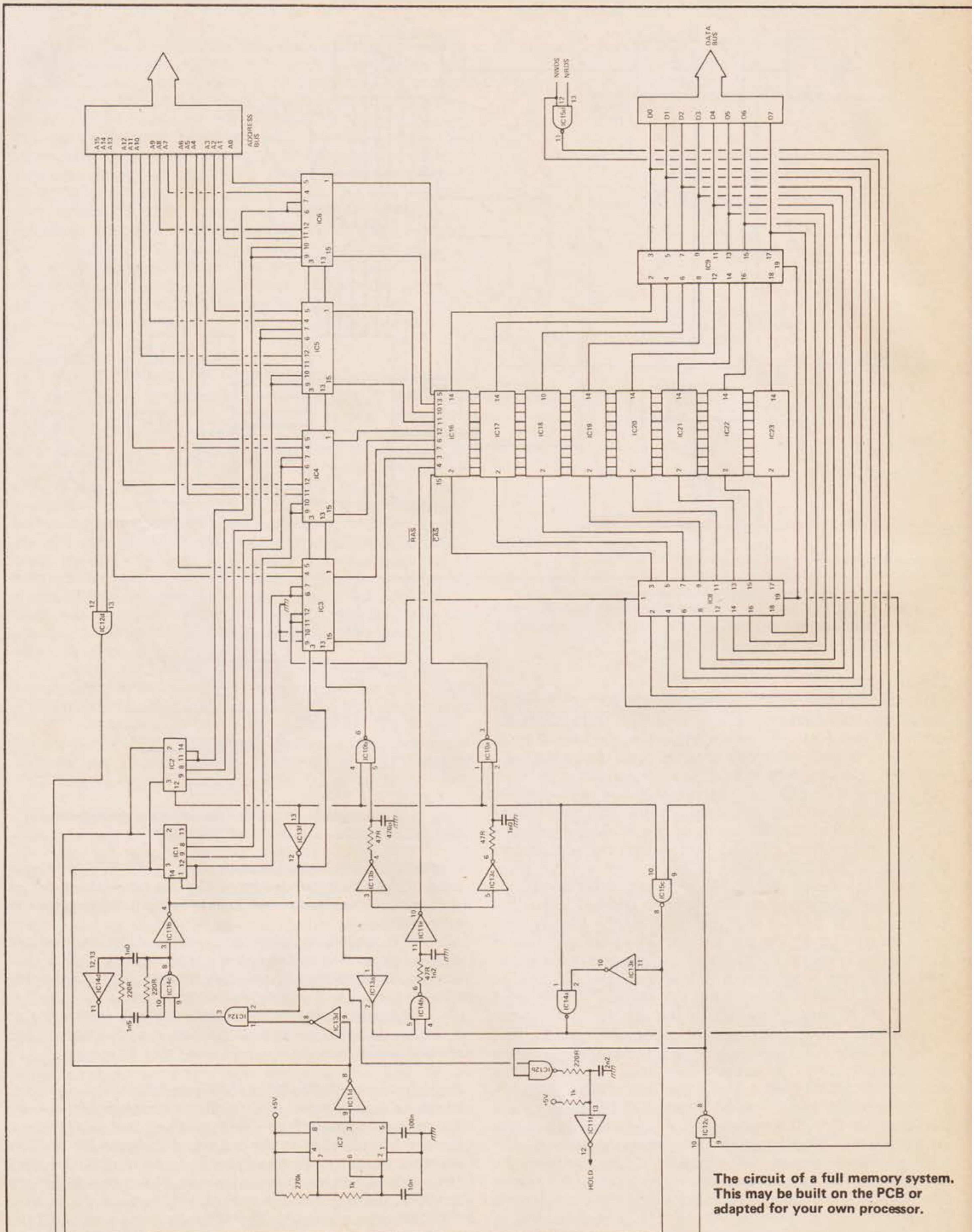
of the 128 row addresses are refreshed by the RAS only method (CAS is inhibited) before the most significant bit of goes high. The circuit then reverts to normal read or write operation.

If the microprocessor attempts to access the memory during refresh it is halted and the read or write cycle is resumed as soon as the burst refresh finishes. The Hold signal remains low until this cycle is complete.

The other gates in the system arbitrate in the case of a request for read or write arriving at the same time as the timer requests a refresh.

**Prototyping Board For Dynamic Memories**

Ideally a double sided printed circuit board should be used for the construction of reliable memories. One way to overcome this problem is to use the board shown in Fig. 4. This has two thirds of its area devoted to housing 32 memory chips that is, the board could contain 64K bytes of memory if the 16384 bit chips are used or 16K bytes if the cheaper 4096 bit ones are preferred. The remaining portion of the board is laid out to accept a wide range of 0.3" and 0.6"




The circuit of a full memory system. This may be built on the PCB or adapted for your own processor.

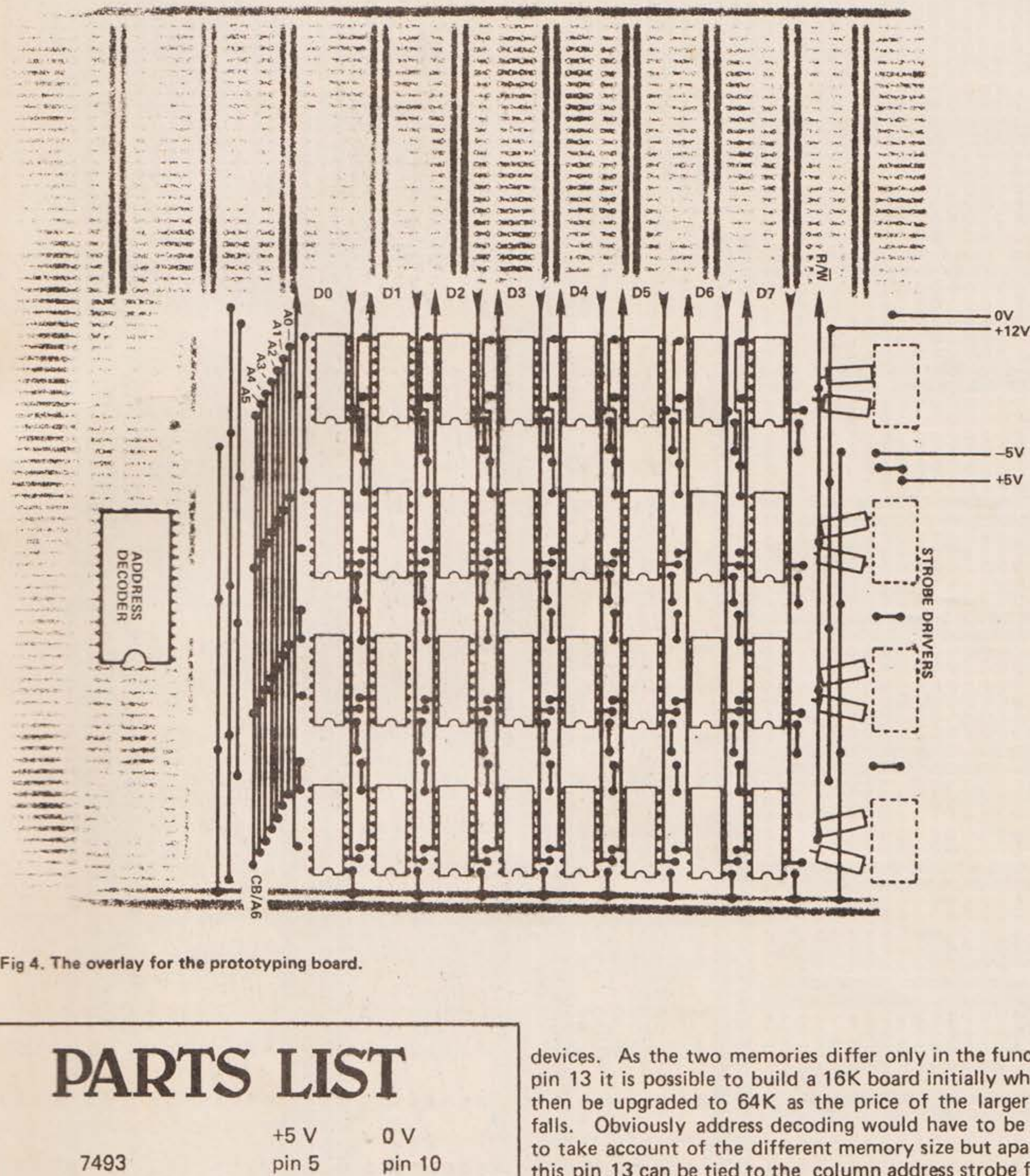



Fig 4. The overlay for the prototyping board.

# PARTS LIST

| | | +5 V | 0 V |
|---|---|---|---|
| IC 1,2 | 7493 | pin 5 | pin 10 |
| IC 3,4,5,6 | 9309 | pin 16 | pin 7 |
| IC 7 | 555 | pin 8 | pin 1 |
| IC 8,9 | 81LS95 | pin 20 | pin 10 |
| IC 10 | 74132 | pin 14 | pin 7 |
| IC 11 | 7414 | pin 14 | pin 7 |
| IC 12 | 7408 | pin 14 | pin 7 |
| IC 13 | 7404 | pin 14 | pin 7 |
| IC 14,15 | 7400 | pin 14 | pin 7 |
| IC 16 – 23 | F16K | pin 9 | pin 16 |

(-5 V pin 1, +12 V pin 8)

devices. As the two memories differ only in the function of pin 13 it is possible to build a 16K board initially which can then be upgraded to 64K as the price of the larger device falls. Obviously address decoding would have to be altered to take account of the different memory size but apart from this pin 13 can be tied to the column address strobe for chip selection (4K chips) but must obviously be used for the most significant address bit in the 16K devices.

Layout is not critical for most of the ancilliary circuitry except for the drivers for address and strobe lines. These drivers should be located at the ends of the arrays as shown in Fig. 5. If the multiplexer/refresh counter (3242) is used this is capable of driving the high capacitance load provided by thirty two devices, otherwise each row of eight should have its own TTL driver. In view of the ease with which it is possible to interchange the 4K and 16K devices it is recommended that the 16K multiplexer/refresh counter (Intel 3242) is used rather than the 4K version (3232) especially as the difference in cost is minimal. In high performance applications where the required cycle time is very short 22

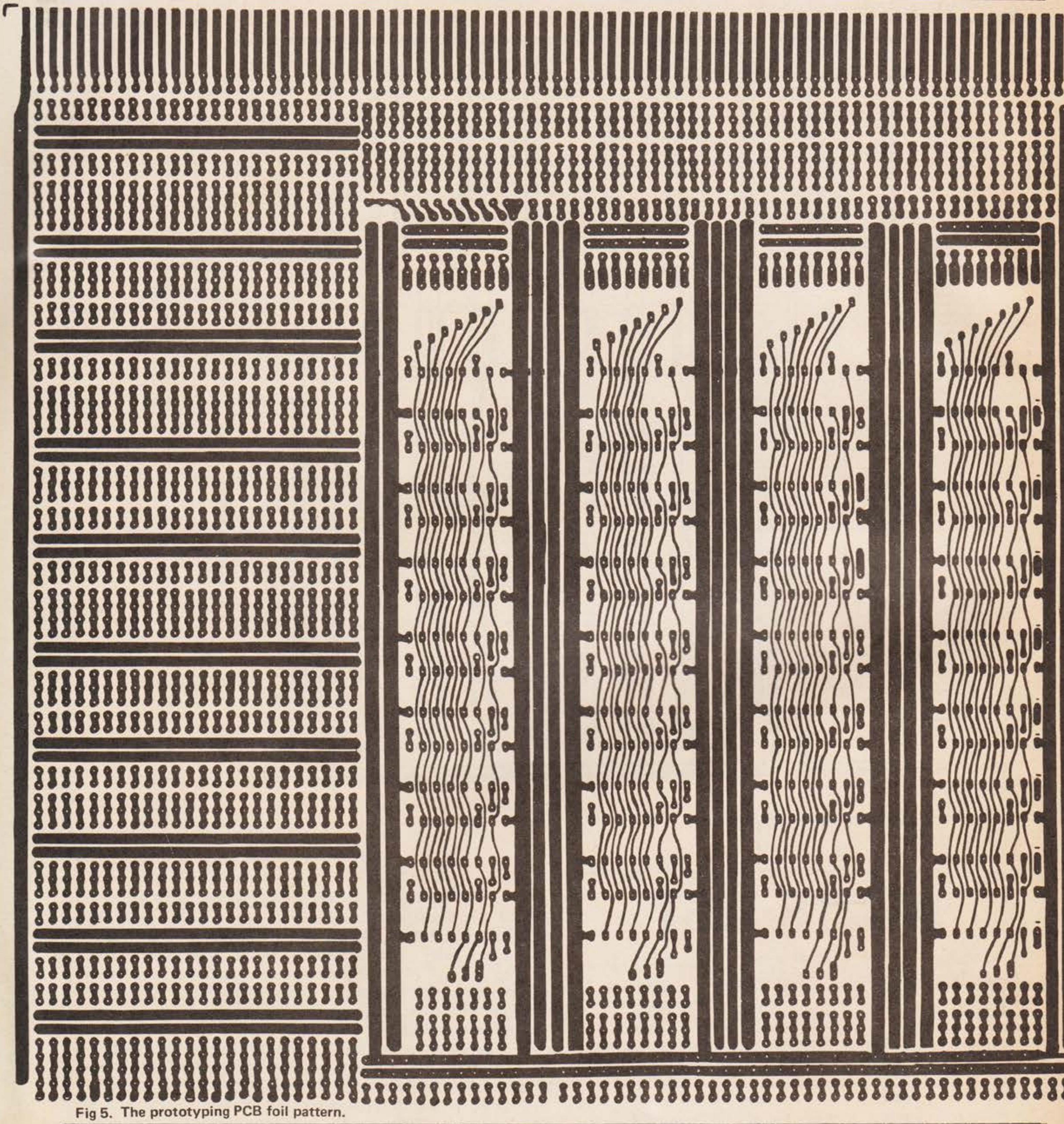


Fig 5. The prototyping PCB foil pattern.

ohm resistors should be put in series with the output of the strobe drivers to reduce transients in these lines (as shown in Fig. 5.).

Care should be taken with decoupling and with the layout of the power supply lines. It is easy to add 0.1 uF ceramic capacitors to decouple the +12 V and –5 V to ground every other device, as close as possible to the pins of the devices. The +5 V supply should be decoupled every eight devices and electrolytic capacitors (4.7 uF) should be used on all three power lines at similar intervals. In addition +12, –5 and O V lines should be strapped by connections not only at each end of the array but at least twice inbet–ween using 0.6mm wire although 0.25mm wire is adequate for the rest of the wiring.

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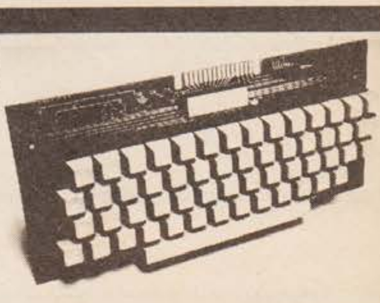

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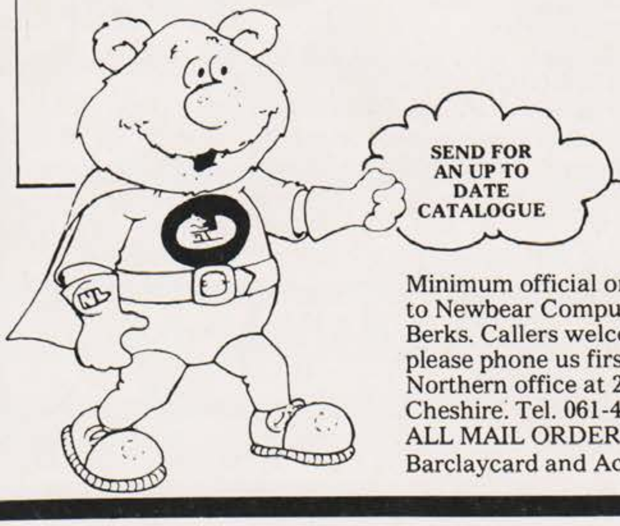


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